ZL30230
Four Channel Universal Clock Generator

Data Sheet

March 2015

Features

- Generates clock signals at power-up per user defined custom OTP (One Time Programmable) configuration
- Dynamically configurable via SPI/I2C interface and volatile configuration registers
- Four independently programmable clock generators output any clock rate from 1 kHz to 750 MHz (precision) / 350 MHz (general purpose)
- Precision clock generators output clocks with jitter below 0.7 ps RMS for 10 G PHYs
- General purpose clock generators output a wide range of digital bus clocks
- Operates from a single crystal resonator, clock oscillator or voltage controlled oscillator
- Supports programmable frequency offsets for clock margining; or for use as a digitally controlled oscillator
- Eight LVPECL outputs; max rate 750 MHz
- Four LVCMOS outputs; max rate 177.5 MHz
- Eight outputs configurable as LVCMOS at 3.3/2.5/1.8 or 1.5 V, max rate160 MHz; or LVDS/LVPECL/HCSL, max rate 350 MHz

Ordering Information

ZL30230GGG2 100 Pin LBGA* 11mmx11mm Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

Applications

- Timing for NPUs, FPGAs, Ethernet switches and PCIe switches
- Timing for 10 Gigabit CDRs, Rapid-IO, PCIe, Serial MII, Star Fabric, Fibre Channel, XAUI
- Processor clock, Processor bus clock, SDRAM clock, DDR clock

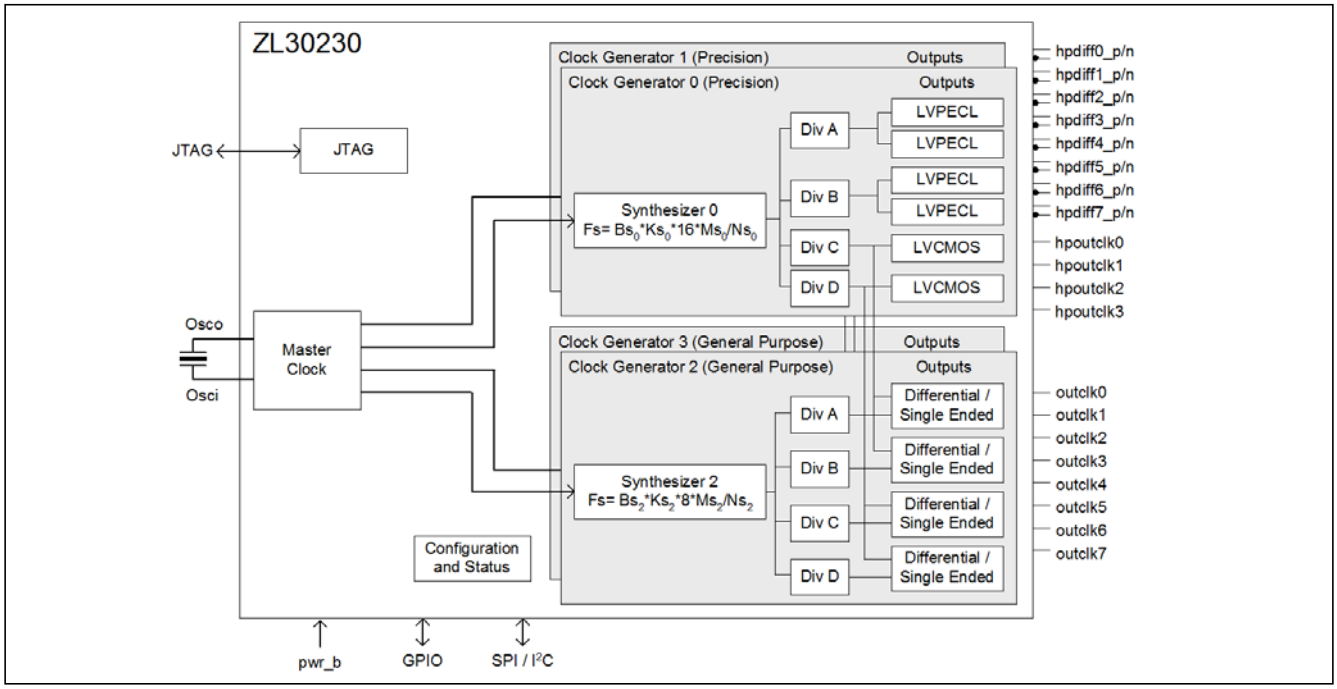

Figure 1 - Functional Block Diagram

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Change Summary

Below are the changes from the June 2012 issue to the March 2015 issue.

Page	Item	Change
1	Ordering Information	Removed ZL30230GGG (leaded version) from the ordering information
23	Custom OTP Configuration	Removed reference to ZLAN-301
118	13.0, “Package Markings“	Added section 13 for package markings

Below are the changes from the January 2012 issue to the June 2012 issue.

Page	Item	Change
36 and 91	Register 0xC6 - Chip_revision_2	Updated chip_revision to 0x03
111	Output to output alignment	Updated limits for $t_{OUT2OUTD}$ to +/- 1 ns

Below are the changes from the December 2011 issue to the January 2012 issue.

Page	Item	Change
31	Procedure for writing registers	Added a new procedure to update registers
32	Reading from Sticky Read registers	Updated Sticky read Procedure
32	Time between two write accesses to the same register	Changed wait time from 200ms to 8ms, added 0x0D as register not requiring wait time
39	Register 0x00 - id_reg	Updated chip_revision bits
39	Register 0x0D - Sticky_r_lock	Updated Description
36, 91	Register 0xC6 - Chip_revision_2	Added register 0xC6

Below are the changes from the July 2011 issue to the December 2011 issue.

Page	Item	Change
32	Reading from Sticky Read registers	Updated Sticky read Procedure
39	Register 0x00 - id_reg	updated ready_indication description
39	Register 0x0D - sticky_r_lock	added register
87	Register 0xB7 - synth2_stop_clock	Bits[3:2] - changed outclk2 to outclk1 Bits[5:4] - changed outclk3 to outclk2
103	Register 0xF7 - spurs_suppression	updated spurs_suppression description
117	Mechanical Drawing	repalced drawing to reflect correct package description

Below are the changes from the June 2011 issue to the July 2011 issue.

Page	Item	Change
1	Feature	OTP feature is added
1, 9,14, 16, 23, 23, 111	All items related the maximum rate of differential output clocks	The maximum rate is updated from 720 MHz to 750MHz
9, 10, 20, 21, 27, 39	All items related waiting time after pwr_b pin goes high during reset procedure	Waiting time after pwr_b pin goes high is changed from 30 ms to 50 ms
14	Section 4.0	Updated for OTP feature
23	Section 5.0	• Section 5.1, 5.1.1, 5.1.2, 5.1.3 and 5.1.4 are updated for three configuration methods:Default configuration, OTP configuration, and SPI/I2C configuration • Original section 5.1.1, 5.1.2, 5.1.3, and 5.1.4 are changed to section 5.2, 5.3, 5.4, and 5.5
31	Section 7.0	For page_register at address 0x7F, there is no waiting time required between two write accesses.
33	Table-5	• Table description is updated for OTP feature • Register 0x01, 0x0E and 0x0F are added • Heading of first column is changed from “Page_Addr” to “Reg_Addr"
39	Section 8.0	Detailed description for new register 0x01, 0x0E, and 0x0F are added
55	Detailed Register Map	"Page_Address" is changed to "Register_Address" for registers which addresses are from 0x80 to 0x91
56	Register synth0_post_div_C	Bit[15:0]: note added for odd post divider
58	Register synth0_post_div_D	Bit[15:0]: note added for odd post divider
61	Register synth1_post_div_C	Bit[15:0]: note added for odd post divider
63	Register synth1_post_div_D	Bit[15:0]: note added for odd post divider
105	DC Electrical Characteristics -Power Core	• "Power for Each Synthesis Engine” is changed to “Current for Each Synthesis Engine” • “PSYN” is changed to “ISYN”
108	DC Electrical Characteristics - High Performance Outputs	Note added for differential output voltage when differential frequency is higher than 720MHz

Page	Item	Change
105	DC Electrical Characteristics	All "AV_{DD-IO}" symbols are replaced with "AV_{DD}"
115	Output Clocks Jitter Generation	Jitter measurement filter for 77.76MHz is changed from "12kHz-5MHz" to "12kHz-20MHz"
116	Section 11.0	Note added for Tjmax

Below are the changes from the January 2011 issue to the June 2011 issue

Page	Item	Change
1	Ordering Information	Corrected package description in ordering information to LBGA.
115	Section 10.1	Section name was renamed to "Output Clocks RMS Jitter Generation".
116	Section 10.2	Table 12 was created for cycle-to-cycle jitter generation.
110	Section 12.0	Replaced drawing to reflect correct package description.

Below are the changes from the November 2010 issue to the January 2011 issue.

Page	Item	Change
6	Figure 2	Names of pin B5, B6, H5, and H6 are changed from AVcore to Vcore
10	Table 1	Names of pin B5, B6, H5, and H6 are changed from AVcore to Vcore, and they are merged to the same entry with pin D5, G5, and G6. Layout application note is referred
25	6.1 Serial Peripheral Interface	SPI burst mode operation description is added
27	Figure 17	Example of a Burst Mode Operation is added
98	Table - Recommended Operating Conditions	Row 2, AVcore is removed from the "Sym" column
104	Table - AC Electrical Characteristics* - Outputs	Row 3, clock duty cycle is changed from "43%-57%" to "45%-55%"
104	Table - AC Electrical Characteristics* - Outputs	Row 4, note "From 0.2AVDD-IO to 0.8AVDD-IO" is removed

1.0 Pin Diagram

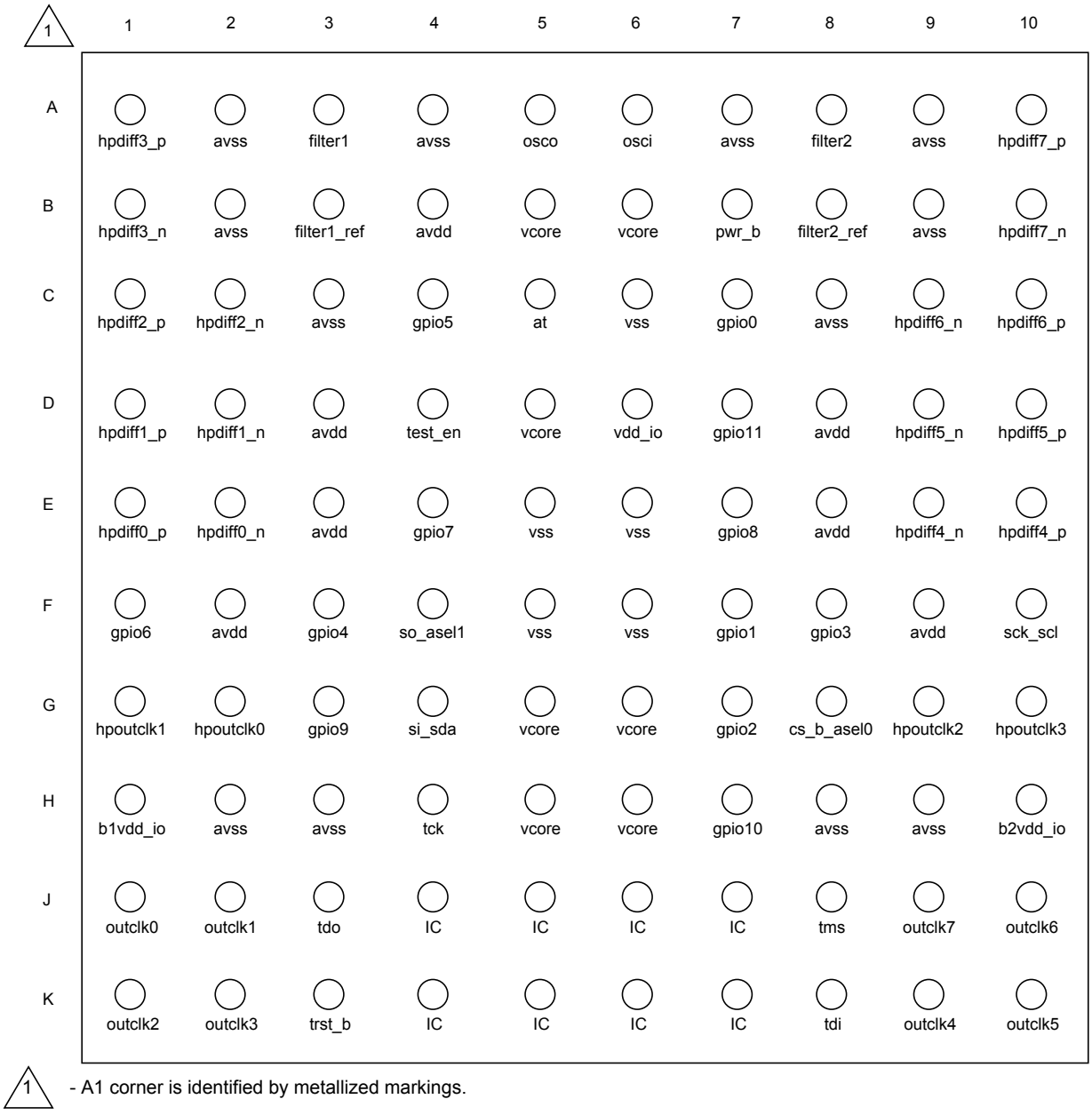


Figure 2 - Package Description

2.0 Pin Description

All device inputs and output are LVCMOS unless it was specifically stated to be differential.

Ball #	Name	I/O	Description
Output Clocks			
J1 J2 K1 K2 K9 K10 J10 J9	outclk0 outclk1 outclk2 outclk3 outclk4 outclk5 outclk6 outclk7	O	**Output Clock 0 to 7.** Configurable output clocks. These can be configured as single ended or differential (0&1, 2&3, 4&5, 6&7) Maximum frequency limit on single ended LVCMOS outputs is 160 MHz, and 350 MHz on differential outputs.
G2 G1 G9 G10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3	O	**High Performance Output Clock 0 to 3.** This output can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
E1 E2 D1 D2 C1 C2 A1 B1 E10 E9 D10 D9 C10 C9 A10 B10	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdif3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdif7_n	O	**High Performance Differential Output Clock 0 to 7 (LVPECL).** This output can be configured to provide any one of the available high performance differential output clocks. Maximum frequency limit on differential outputs is 750 MHz
Control and Status			
B7	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The pwr_b pin should be held low for 2 ms. Following a reset, the input reference source and output clocks are phase aligned. This pin is internally pulled-up to V_{DD}. **User can access device registers either 50 ms after pwr_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling the register at address 0x00.**

Table 1 - Pin Description

Ball #	Name	I/O	Description
C7 F7 G7 F8 F3 C4 F1 E4 E7 G3 H7 D7	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6 gpio7 gpio8 gpio9 gpio10 gpio11	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Other status and control pins could be muxed to become part of the available GPIO pins. Recommended usage of GPIO include: • Differential output clock enable (per output or as a bank of 2 or 4 outputs) • High performance LVCMOS outputs enable • Microport interface protocol I2C or SPI • Master Clock frequency rate Pins 5:0 are internally pulled down to GND and pins 11:6 are internally pulled up to V_{DD}. If not used GPIO can be kept unconnected. **After power on reset, device GPIO[0,1,3,4,5] configure some of device basic functions, GPIO[3] set I2C or SPI control mode, GPIO[1,0] set master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 50 ms after reset, and released and used for normal GPIO functions.** **The GPIO[4,5] pins must be either pulled low with external 1KΩ resistors; or they must be driven low for 50 ms after reset, and then released and used for normal GPIO functions.**
Host Interface			
F10	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}.
G4	si_sda	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
F4	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.
G8	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode.This pin is internally pulled up to V_{DD}.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
APLL Loop Filter			
A3	filter1	A	**External Analog PLL1 Loop Filter terminal.**
B3	filter1_ref	A	**Analog PLL1 External Loop Filter Reference.**
A8	filter2	A	**External Analog PLL2 Loop Filter terminal.**
B8	filter2_ref	A	**Analog PLL2 External Loop Filter Reference.**
JTAG (IEEE 1149.1) and Test			
D4	test_en	I	**Test Mode Enable.** A logic high at this pin enables device test modes. This pin is internally pulled down to GND. Connect this pin to GND.
C5	at	A-I/O	**Analog PLL Test.** Test pin for analog PLL.
J3	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K8	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
K3	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H4	tck	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
J8	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
A5	osco	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osci. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected.
A6	osci	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osco. For clock oscillator operation, this pin is connected to a clock source.
Miscellaneous			
J4 K4 J5 K5 K6 J6 K7 J7	IC		**Internal Connect.** Connect to GND.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
Power and Ground			
D6	V_{DD-IO}		**Positive Supply Voltage IO.** 3.3V_{DC} nominal.
H1	B1V_{DD-IO}		**Bank 1 Positive Supply Voltage IO.** Output group specific +3.3/2.5/1.8/1.5V_{DC} nominal.
H10	B2V_{DD-IO}		**Bank 2 Positive Supply Voltage IO.** Output group specific +3.3/2.5/1.8/1.5V_{DC} nominal.
B5 B6 D5 G5 G6 H5 H6	V_{CORE}		**Positive Supply Voltage.** +1.8V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-269 for recommendations
B4 D3 D8 E3 E8 F2 F9	AV_{DD}		**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
C6 E5 E6 F5 F6	V_{SS}		**Ground.** 0 Volts.
A2 A4 A7 A9 B2 B9 C3 C8 H2 H3 H8 H9	AV_{SS}		**Analog Ground.** 0 Volts.

Table 1 - Pin Description (continued)

3.0 Application Example

The device has multiple independent clock synthesizers, all locked to the external xtal or oscillator. The device will generate all the clocks that drive the different components on the PCB.

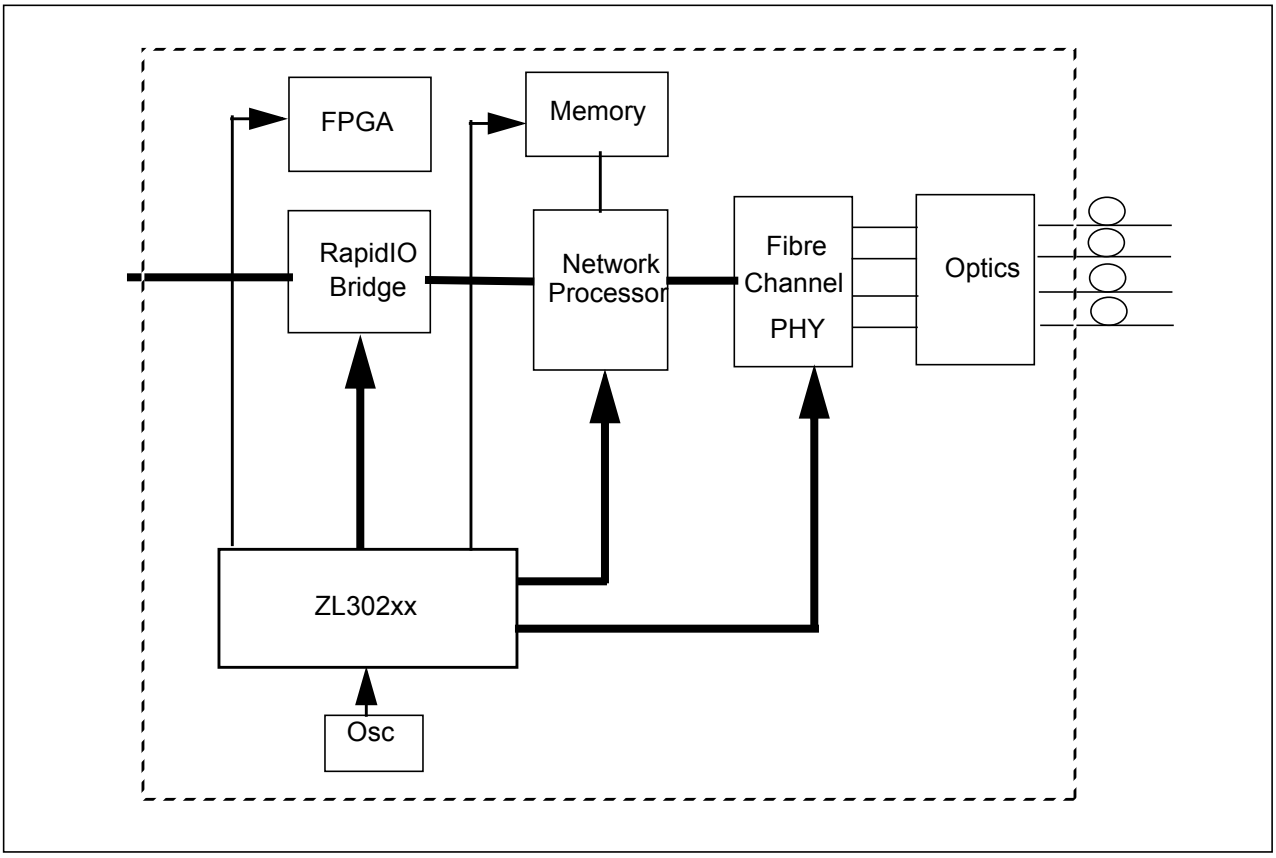


Figure 3 - Application Diagram

4.0 Functional Description

The functional block diagram of the ZL30230 is shown in Figure 1.

The ZL30230 is a programmable clock generator that can be configured by any of the following methods: power-up with its default configuration; power-up with a custom OTP (One Time Programmable) configuration; after power-up it can be dynamically configured via the SPI/I2C port. Configurations set via the SPI/I2C port are volatile and will need to rewritten if the device is reset or powered-down. The SPI/I2C port is also used to access the status registers.

The ZL30230 has four independently programmable clock generators. Two of the clock generators output precision clocks of up to 750MHz with jitter below 0.7ps RMS; and two of the clock generators output general purpose clocks of up to 350MHz with jitter below 20ps RMS. The ZL30230 uses a single master clock based on a crystal resonator, a clock oscillator or a voltage controlled oscillator. All of the clocks output by the ZL30230 will have the same PPM (Parts Per Million) frequency accuracy as the master clock source.

The ZL30230 precision synthesizers can be programmed to generate any frequency between 1,000MHz and 1,500MHz; and the general purpose synthesizers can be programmed to generate any frequency between 500MHz and 750MHz. The frequency resolution of the synthesizers is much less than 1 PPB (Parts Per Billion).

Each synthesizer is followed by four independently programmable 23 bit even/odd post dividers. For skew management purposes, the post dividers feeding the single ended or configurable outputs can impose a phase shift on their output clock signals with resolution equal to a single period of their respective synthesizers' clocks.

All of the ZL30230 clock generators have the same PPM frequency accuracy as the master clock source and therefore the frequency relationships between the clock generators can be programmed exactly. It is possible, for example, to have one generator output 625MHz for 10GBASE-T while another generator outputs 625MHz * 66/64 * 255/237 for 10GBASE-T over OTN (Optical Transport Network). The clock generators will not drift or slip with respect to each other.

Clocks from the two precision clock generators can be output on LVPECL or LVCMOS outputs, and they can be routed to configurable outputs that can be differential (LVPECL, LVDS, or HCSL) or single ended (LVCMOS or LVTTL) with programmable slew rates.

Clocks from the two general purpose clock generators can be output on configurable outputs that can be differential (LVPECL, LVDS, or HCSL) or single ended (LVCMOS or LVTTL); the single ended outputs have programmable slew rates.

The ZL30230 provides ten GPIO pins that can be used as enable pins for the hpout and hpdiff outputs; they can also be used enable or stop the output clocks from the post dividers on a falling or rising edge.

The detailed operation of the ZL30230 is described in the following sections.

4.1 Frequency Synthesis Engine

The device frequency synthesis engine is comprised of a hardware DCO and an analog jitter filtering APLL with built-in digital jitter attenuation scheme. It has two ultra low jitter frequency synthesis engines that can generate output clocks which meet the jitter generation requirements detailed in section 10.0, “Performance Characterization“.

4.2 Dividers and Skew Management

The device has 4 independent dividers associated with each frequency synthesis engine.

The divider engines associated with the high performance differential outputs generate output clocks between 1 kHz and 750 MHz with 50% duty cycle. The other divider engines generate output clocks between 1 kHz and 177.5 MHz for high performance LVCMOS outputs and 160 MHz for single ended configurable outputs with 50% duty cycle. When configurable outputs are in differential mode, the maximum frequency is 350 MHz.

The divider modules generating the single ended output clocks provides the ability to manage the phase skew of the output clock by a coarse step equal to the internal high speed clock period.

The single ended generated output clocks can be stopped either on rising or falling edge (programmed through serial interface or GPIO).The device can be configured to adjust the phase skew of single ended clocks in steps of sub high speed synthesizer clock cycle.

4.3 Output Multiplexer

Figure 4 shows the multiplexing configuration supported.

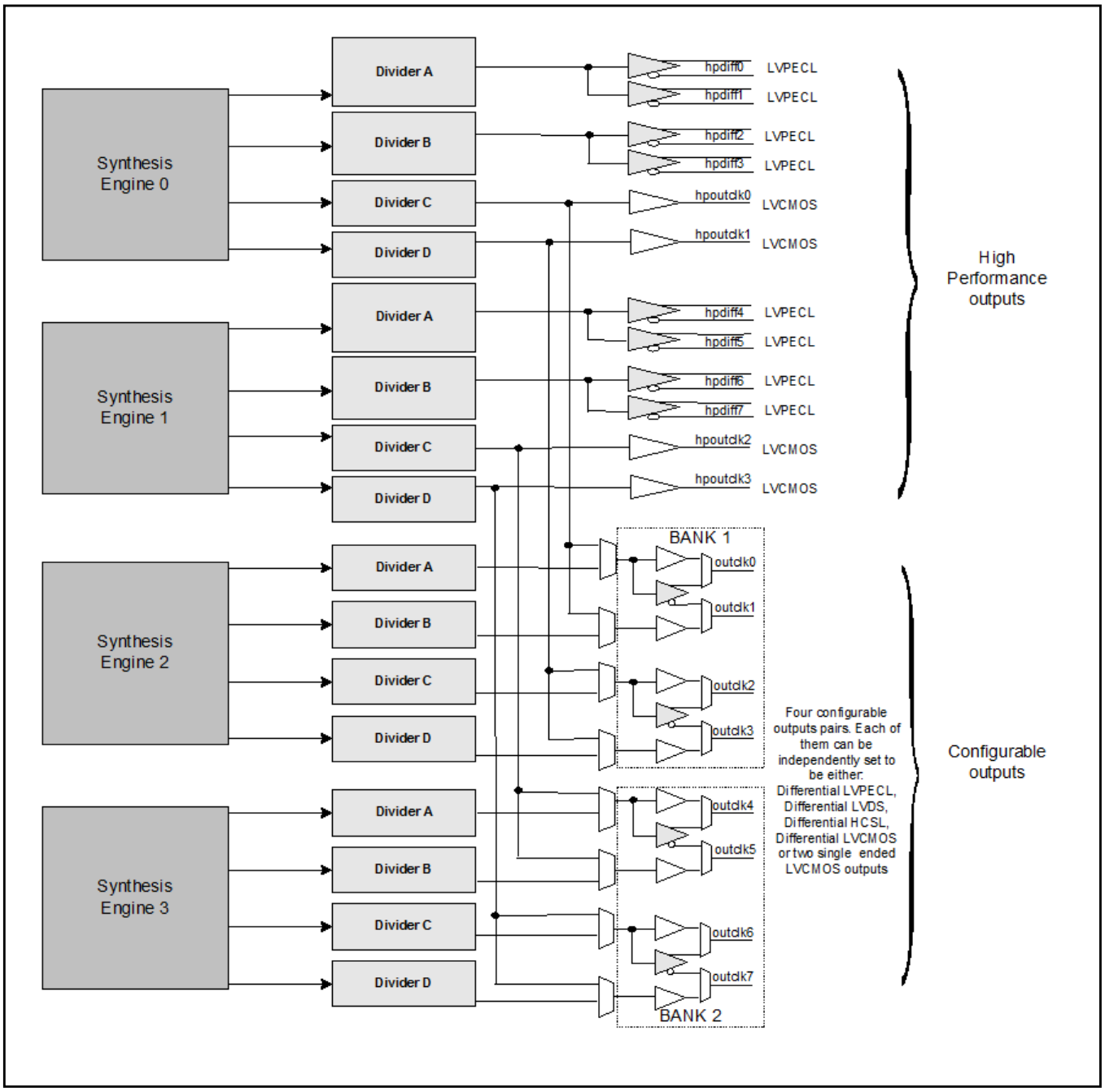


Figure 4 - Output Clock Muxing Configuration

4.4 Output Drivers

The device has 8 high performance (HP) differential (LVPECL) outputs.

The device has 4 high performance (HP) single ended (LVCMOS) outputs.

The device also has 2 banks of configurable output drivers. Each bank can be set as a 4 single ended drivers (LVCMOS or LVTTL) or as a 2 differential output drivers (LVPECL, LVDS, HSTL or HCSL). Each output bank has its own power supply pins, such that each bank of 4 single ended drivers can be set to operate in 3.3 V, 2.5 V, 1.8 V or 1.5 V mode.

High Performance (HP) single ended driver (LVCMOS) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 177.5 MHz.

The high performance (HP) differential driver (LVPECL) supports the jitter specification detailed in section 10.0, “Performance Characterization“ and a maximum speed of 750 MHz.

LVPECL outputs should be terminated as shown in Figure 5. Terminating resistors provide 50 Ω equivalent Thevenin termination as well as biasing for the output LVPECL driver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

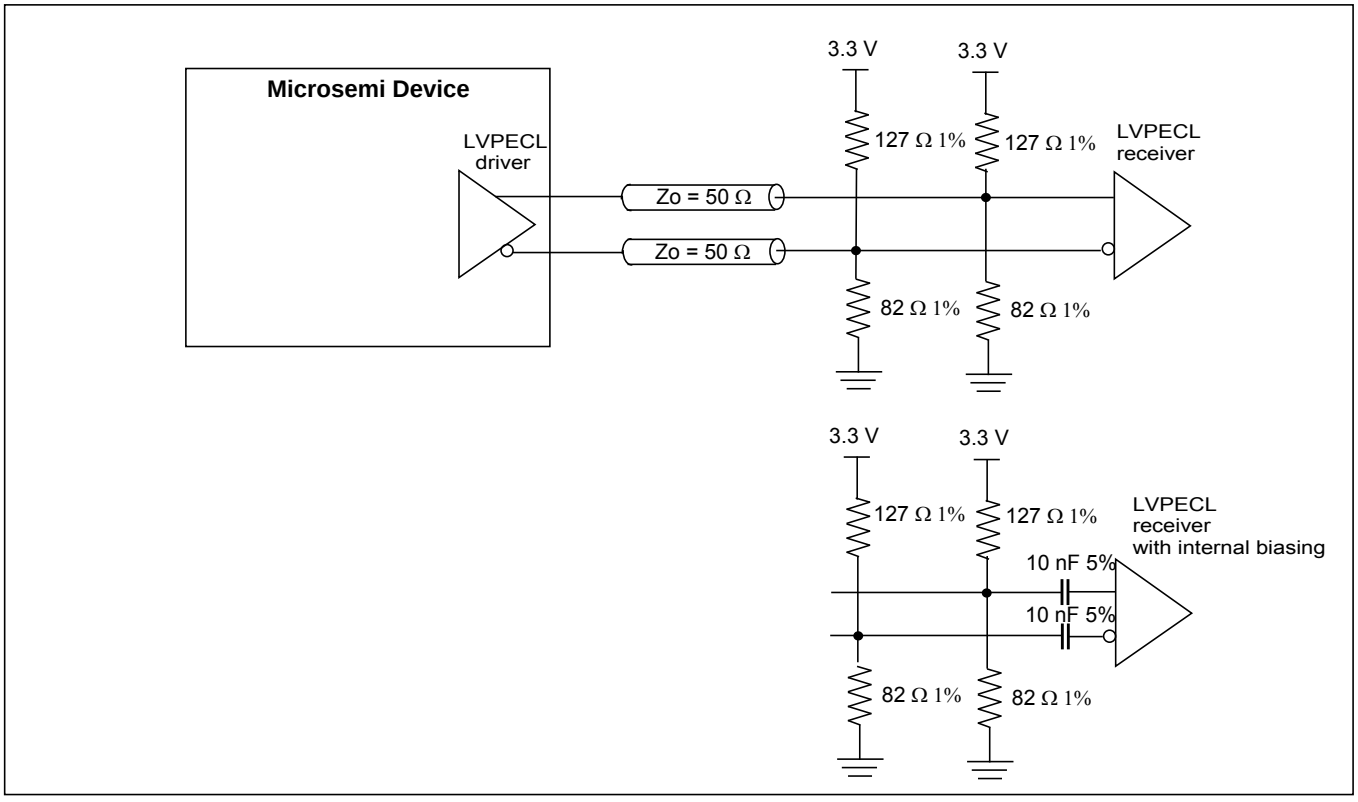


Figure 5 - Terminating LVPECL Outputs

If the transmission line is required to be AC coupled then the termination shown in Figure 6 should be implemented. 200 Ω resistors are used to provide DC biasing for LVPECL driver. Both AC coupling capacitor and biasing resistors should be placed as close as possible to output pins.

Thevenin termination (127 Ω and 82 Ω resistors) provide 50 Ω termination as well as biasing of the input LVPECL receiver. If the LVPECL receiver has internal DC biasing then the line should be terminated with 100 Ω termination resistor between positive and negative input. In both cases termination resistors should be places as close as possible to the LVPECL receiver pins. Some LVPECL receivers have internal biasing and termination. In this case no external termination should be present.

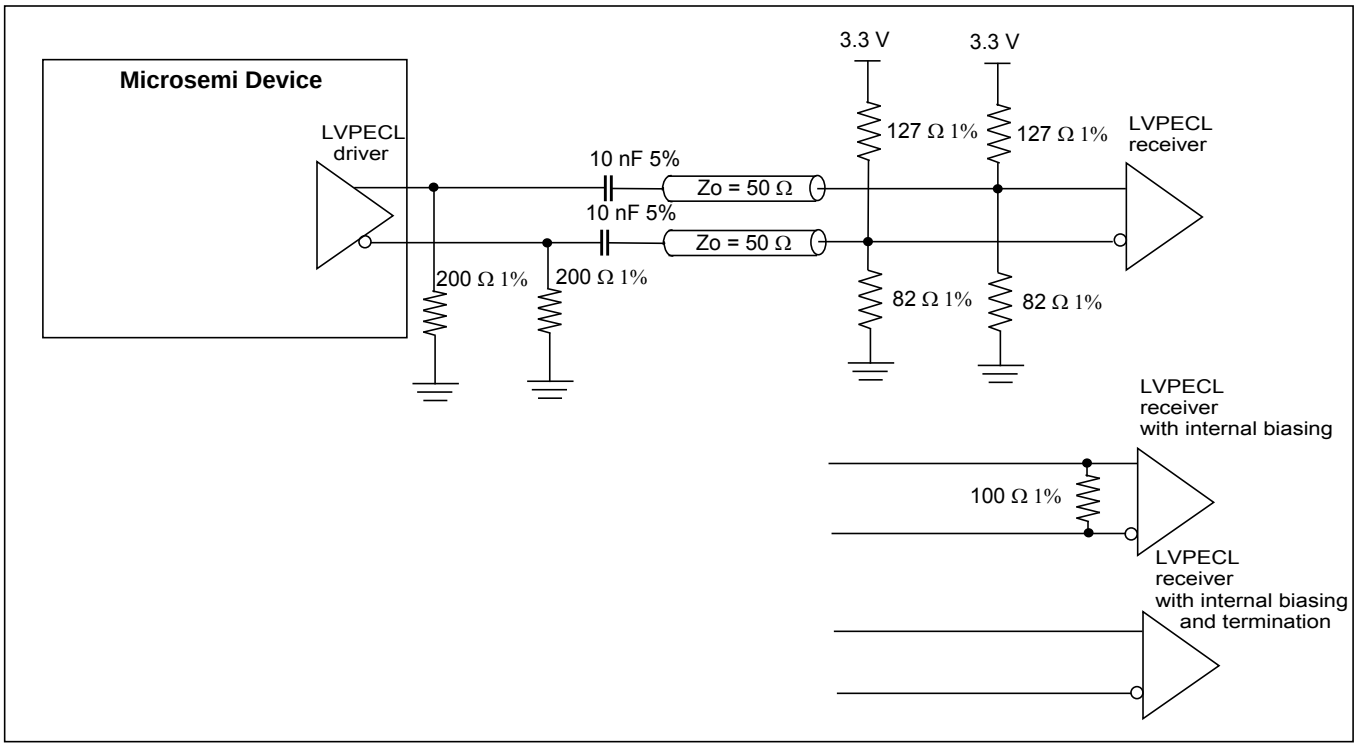


Figure 6 - Terminating AC coupled LVPECL Outputs

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 7. The same type of termination should be used for configurable outputs when they are set to be LVCMOS.

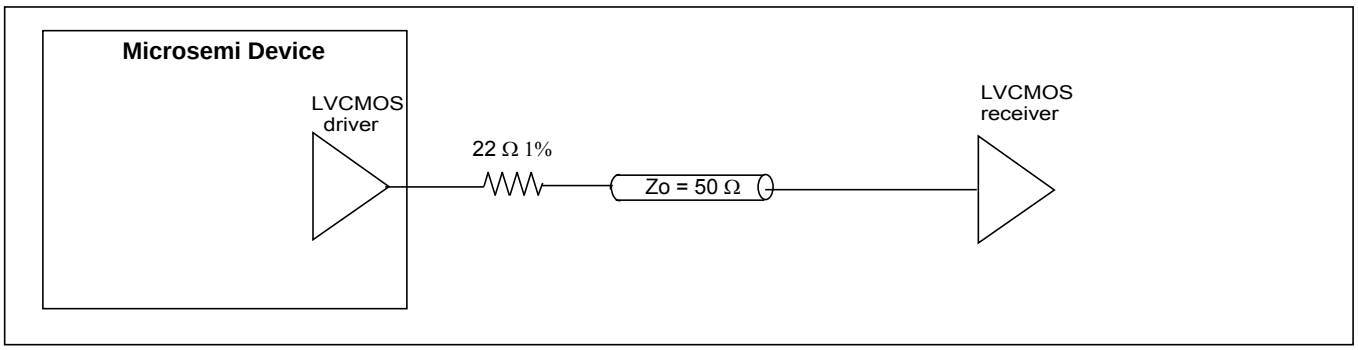


Figure 7 - Terminating LVCMOS Outputs

If the configurable output drivers are programmed to be LVDS, the termination in Figure 8 should be used.

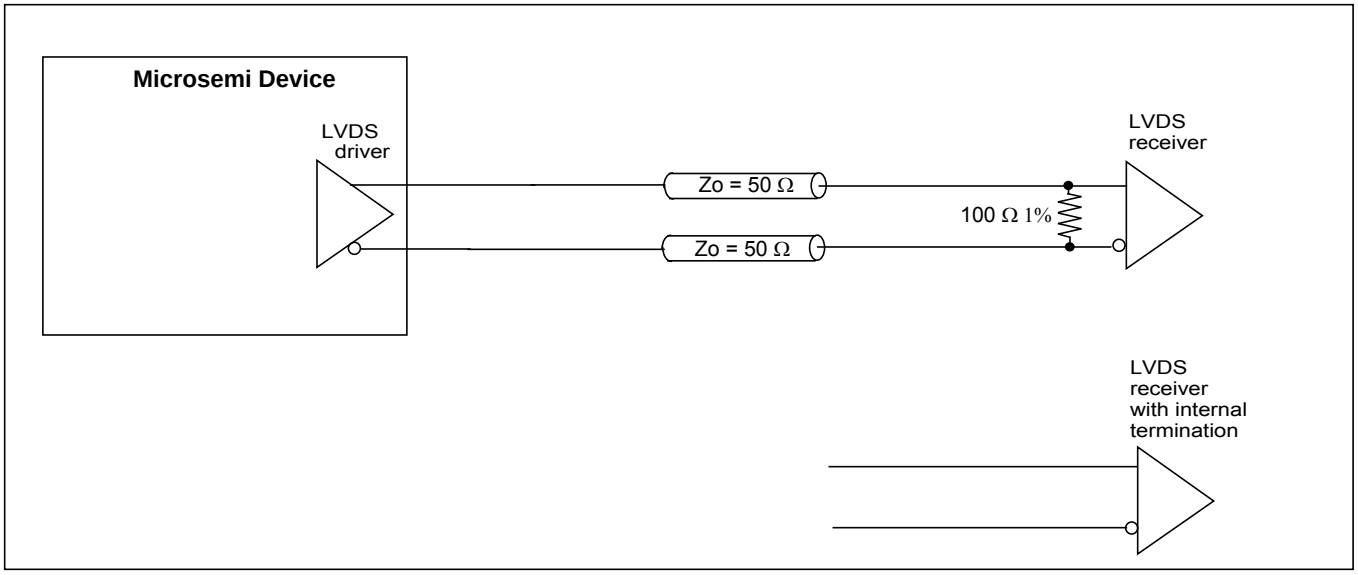


Figure 8 - Terminating LVDS Outputs

When configurable outputs are set to be HCSL, the termination shown in Figure 9 should be used.

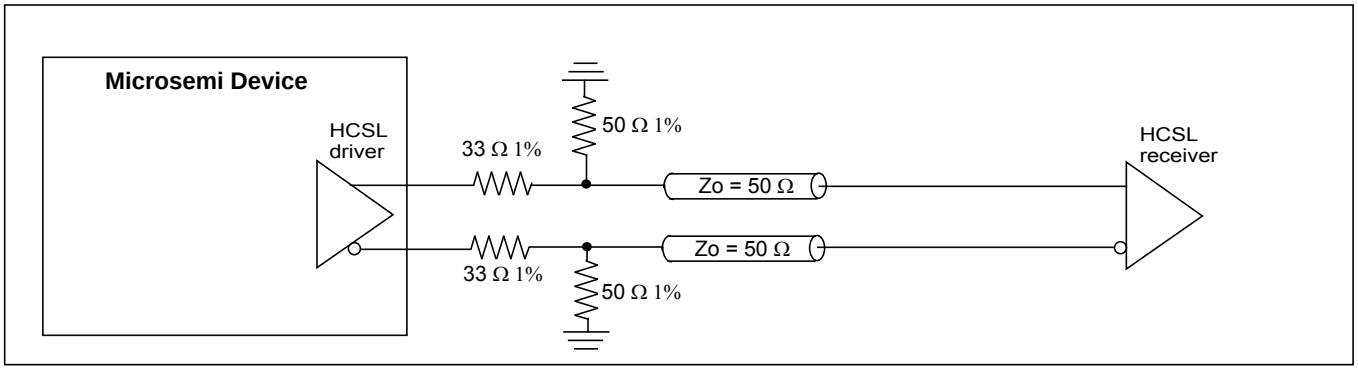


Figure 9 - Terminating HCSL Outputs

4.4.1 Programmable Single Ended Driver - Slew Rate Control

The following are the motivation for fast slew rate:

- Buffer high speed single ended (CMOS) output clock (up to 160 MHz) and/or
- Buffer single ended (CMOS) output clock on a large output load (up to 30 pf)
- Provide rail to rail single ended output clock for any selection of output drive supply voltage (1.5, 1.8, 2.5, 3.3 Volt)

Motivation for medium slew rate:

- Maintain limited output clock ringing and PCB output clocks cross modulation when driving low speed output clock or when small load is present at the output

Each of the available single ended output of the device has 2 available slew rate control limits.These limits are user selectable based on: output clock speed, expected output load or output supply voltage. Table 2 details the limits and the expected output clock slew rates.

	Slew Rate for Fast Slew		**Slew Rate for Medium Slew**	
Expected Load	10 pF	20 pF	10 pF	20 pF
Output Clock 80 MHz or less	1.62 V/ns	1.47 V/ns	0.93 V/ns	0.96 V/ns
Output Clock 160 MHz or less	1.58 V/ns	1.38 V/ns	1.09 V/ns	1.08 V/ns

Table 2 - Slew Rate Control Limits Versus Output Clock Rise/Fall Times

4.5 Master Clock Interface

The master oscillator determines the device free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to Application Note ZLAN-68 for a list of recommended clock oscillators and crystals.

4.6 Clock Oscillator and Crystal Circuit

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 10. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

When using crystal resonator as the master timing source, connect crystal between **osci** and **osco** pins as shown in Figure 10. Crystal should have bias resistor of 1MΩ and load capacitances C1 and C2. Value of load capacitances is dependent on crystal and should be as per crystal datasheet. Crystal should be a fundamental mode type -- not an overtone. See ZLAN-68 for crystal recommendation.

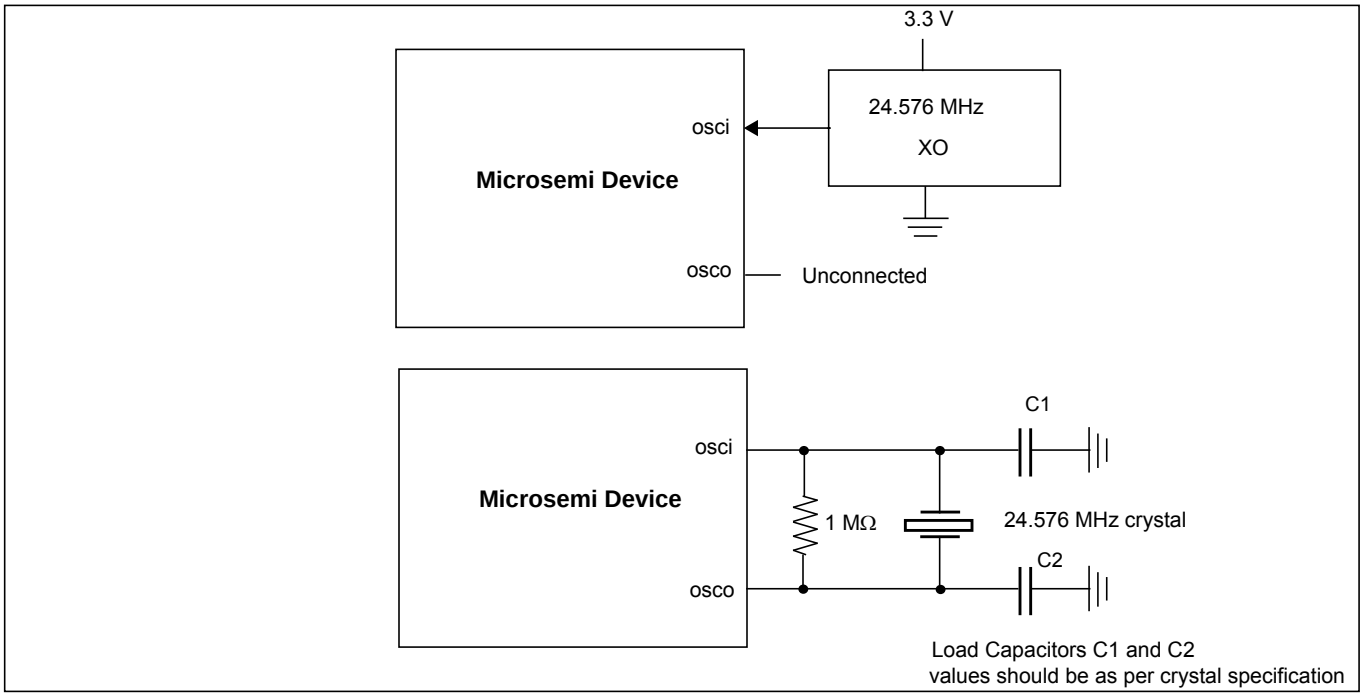


Figure 10 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the available GPIO pins, right after pwr_b get de-asserted. To select 24.576 MHz oscillator, GPIO[1:0] pins need to be held high for 50 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO. Alternatively, these pins can be pulled high with 1 KΩ resistors.

GPIO [1:0]	Master Clock Frequency
0	reserved
1	reserved
2	reserved
3	24.576 MHz

Table 3 - Master Clock Frequency Selection

4.7 Power Up/Down Sequence

The 3.3 V supply should be powered before or simultaneously with the 1.8 V supply. The 1.8 V supply must never be greater than the 3.3 V supply by more than 0.3V. The 1.5V/1.8V/2.5V/3.3V configurable output supply must never be greater than the 3.3 V supply by more than 0.3 V.

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.8 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Application Note ZLAN-269.

4.9 Power on Reset and Initialization Circuit

To ensure proper operation, the device must be reset by holding the pwr_b pin low for at least 2 ms after power-up when 3.3 V and 1.8 V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 11. This circuit provides approximately 2 ms of reset low time. The pwr_b input has Schmidt trigger properties to prevent level bouncing.

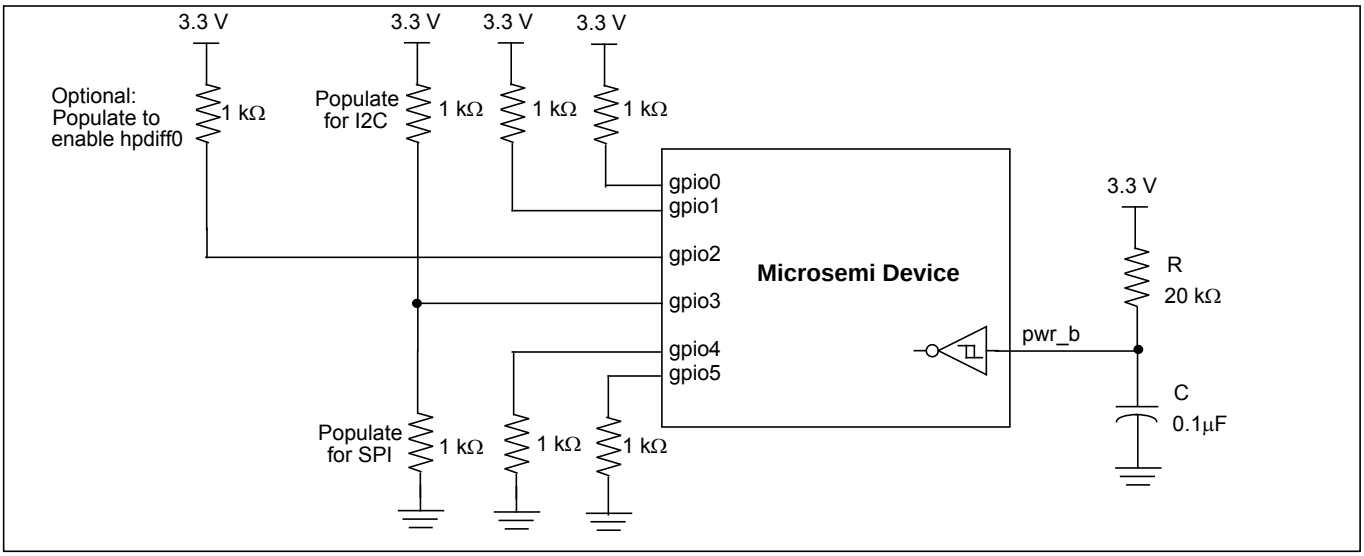


Figure 11 - Typical Power-Up Reset and Configuration Circuit

General purpose pins gpio[0,1,3,4,5] are used to configure device on the power up. They have to be pulled up/down with 1 KΩ resistors as shown in Figure 11 or they can be pulsed low/high during the pwr_b low pulse and kept at the same level for at least 50 ms after pwr_b goes high. After 50 ms they can be released and used as general purpose I/O as described in Section 5.0.

By default all outputs are disabled to allow user first to program required frequencies for different outputs and then to enable corresponding outputs. During the prototype phase, hardware designer can verity if the device is working properly even before software driver is implemented just by pulling up gpio2 pin which enables hpdiff0 output (generates 622.08 MHz by default).

4.10 Ultra Low Jitter Synthesizer Filter Components and Recommended Layout

The low jitter APLL has an on-chip loop filter, but for optimal APLL jitter performance external loop filter is recommended, the following component values are recommended:

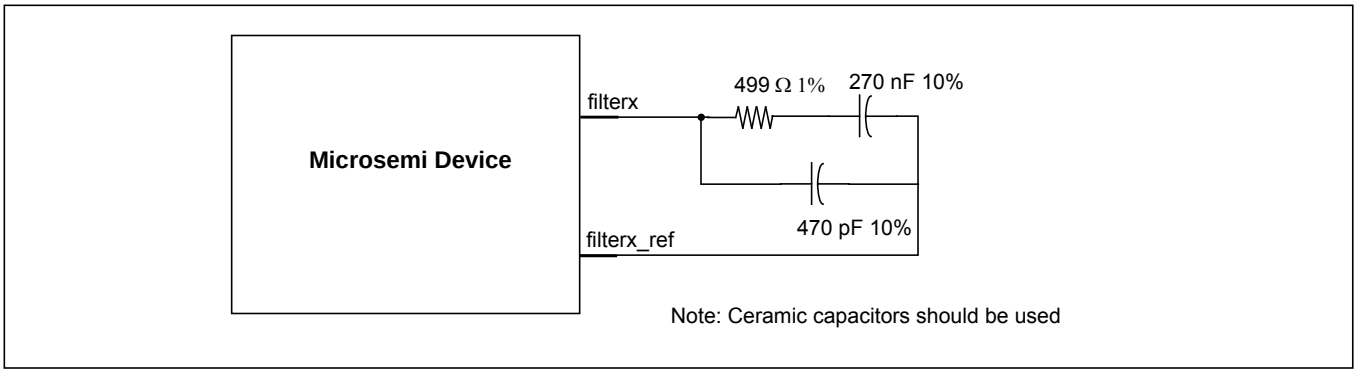


Figure 12 - APLL Filter Component Values

Recommended layout for loop filters is shown in Figure 13:

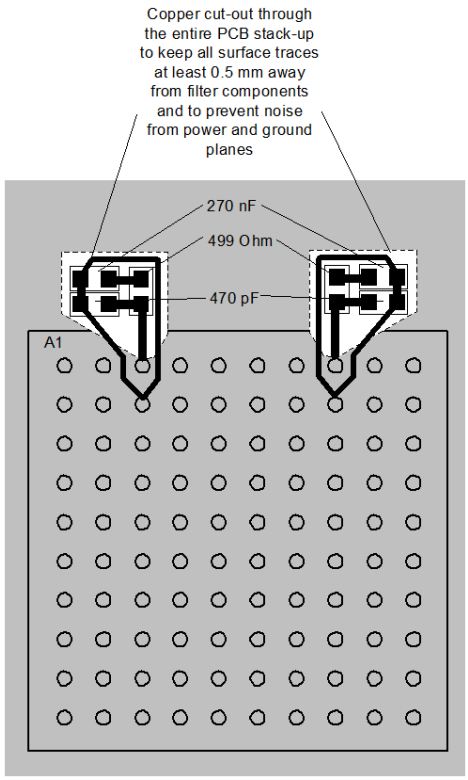


Figure 13 - Recommended Layout for Loop Filters

5.0 Configuration and Control

5.1 Configuration Registers

The ZL30230 configuration is composed of 253 x 8 bits. The configuration registers are assigned their values by any of the following three methods:

1) Default configuration
2) Custom OTP (One Time Programmable) configuration
3) SPI/I2C configuration

5.1.1 Default Configuration

At power-up the device sets its configuration registers to the default reset values.

5.1.2 Custom OTP Configuration

At power-up the device sets it configuration registers to the user defined custom configuration values stored in its one time programmable memory. Custom configurations can be generated using Microsemiès Clockcenter GUI (ZLS30CLKCTR). For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.1.3 SPI/I2C Configuration

After power-up the values of R/W type configuration registers can be dynamically written via the SPI/I2C port. Configurations set via the SPI/I2C port are volatile and will need to rewritten if the device is reset or powered-down.

5.2 Output Multiplexer Configuration and Programmability

The following is the set of parameters that are configurable:

- Output multiplexer configuration
- Start or Stop clock.

5.3 Synthesizers Configuration and Programmability

The following is the set of parameters that are configurable:

- Synthesizer 0 and 1 output frequency between 1.0 GHz and 1.5 GHz
- Synthesizer 2 and 3 output frequency between 500 MHz and 750 MHz.
- Synthesizers 0, 1, 2, 3 high speed output clock, defined as a 1 kHz multiple and 1 kHz multiple with M/N ratio

5.4 Output Dividers and Skew Management Configuration and Programmability

The following is the set of parameters that are configurable:

- Post divider enable/disable
- Divider ratio (2 different setting, independent for each one of the divider outputs)
- Output phase shift value (skew)

5.5 Output Drivers configuration and Programmability

The following is the set of parameters that are configurable:

- Output driver Enable/Disable
- Output driver mode (single ended or differential)

- Single ended driver slew rate control (medium and fast)
- Differential driver mode (LVPECL)

5.6 GPIO Configuration and Programmability

The device GPIO is mapped by the SPI/I2C programmability. The following is an example of control signals that can be supported:

- Differential output clock enable (per output or as a bank of 2 or 4 outputs)
- Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR).
- Output clock stop/start
- Microport Interface Protocol I2C or SPI

The following table defines the function of the GPIO pin when configured as a control pin. Configuring the value in bit 6:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Default		
0x00	default	GPIO pin defined as an input and no function assigned to it.
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer0 Post Divider C bit1	This signal is OR-ed with the 'Syntheizer0 Post Divider C stop clock' bit1 in the 'Synthesizer0 and Synthesizer1 Post Dividers stop clock' register.
0x45	Stop output clock from Synthesizer0 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x46	Stop output clock from Synthesizer0 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x47	Stop output clock from Synthesizer0 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4C	Stop output clock from Synthesizer1 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4D	Stop output clock from Synthesizer1 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4E	Stop output clock from Synthesizer1 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4F	Stop output clock from Synthesizer1 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1

Value	Name	Description
0x50	Stop output clock from Synthesizer2 Post Divider A bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x51	Stop output clock from Synthesizer2 Post Divider A bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x52	Stop output clock from Synthesizer2 Post Divider B bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x53	Stop output clock from Synthesizer2 Post Divider B bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x54	Stop output clock from Synthesizer2 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x55	Stop output clock from Synthesizer2 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x56	Stop output clock from Synthesizer2 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x57	Stop output clock from Synthesizer2 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x58	Stop output clock from Synthesizer3 Post Divider A bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x59	Stop output clock from Synthesizer3 Post Divider A bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5A	Stop output clock from Synthesizer3 Post Divider B bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5B	Stop output clock from Synthesizer3 Post Divider B bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5C	Stop output clock from Synthesizer3 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5D	Stop output clock from Synthesizer3 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1

Value	Name	Description
0x5E	Stop output clock from Synthesizer3 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5F	Stop output clock from Synthesizer3 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
High Performance Differential Outputs		
0x60	Enable Differential output HPDIFF0	This signal is OR-ed with the 'Enable HPDIFF0' bit in the 'High performance differential output enable' register. Functionality of this signal is explained in hpdiff_en register.
0x62	Enable Differential output HPDIFF1	Same description as Enable Differential output HPDIFF0
0x64	Enable Differential output HPDIFF2	Same description as Enable Differential output HPDIFF0
0x66	Enable Differential output HPDIFF3	Same description as Enable Differential output HPDIFF0
0x68	Enable Differential output HPDIFF4	Same description as Enable Differential output HPDIFF0
0x6A	Enable Differential output HPDIFF5	Same description as Enable Differential output HPDIFF0
0x6C	Enable Differential output HPDIFF6	Same description as Enable Differential output HPDIFF0
0x6E	Enable Differential output HPDIFF7	Same description as Enable Differential output HPDIFF0
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the 'High performance CMOS output enable' register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0
0x74	Enable HPOUTCLK2	Same description as Enable HPOUTCLK0
0x76	Enable HPOUTCLK3	Same description as Enable HPOUTCLK0

6.0 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I^2C interface. The type of interface is selected using the startup state of the GPIO pins.

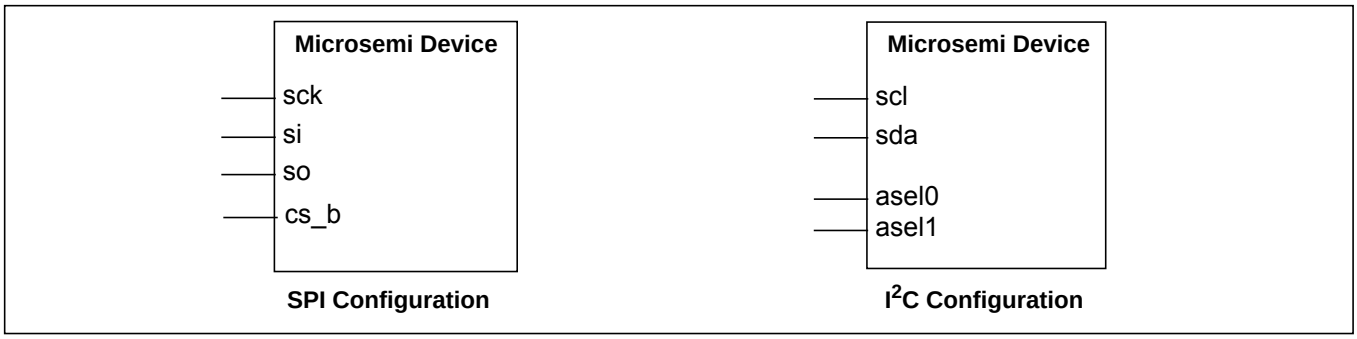


Figure 14 - Serial Interface Configuration

The selection between I2C and SPI interfaces is performed at start-up using GPIO[3] pin, right after pwr_b gets de-asserted. The GPIO pin need to be held at their appropriate value for 50 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO.

Both interfaces use seven bit address field and the device has eight bit address space. Hence, memory is divided in two pages. Page 0 with addresses 0x00 to 0x7E and Page 1 with addresses 0x80 to 0xFF. Writing 0x01 to Page Register at address 0x7F, toggles SPI/I2C accesses between Page 0 and Page 1.

GPIO[3]	Serial Interface
0	SPI
1	I2C

Table 4 - Serial Interface Selection

6.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs**_**b**_asel0 pin is active. If the **sck**_scl pin is low during **cs**_**b**_asel0 activation, then MSB first timing is selected. If the **sck**_scl pin is high during **cs**_**b**_asel0 activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs**_**b**_asel0 is high. During SPI access, the **cs**_**b**_asel0 pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs**_**b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so**_asel1 pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 15, Figure 16 and Figure 17. Timing characteristics are shown in Table 6, Figure 26, and Figure 27.

6.1.1 Least Significant Bit (LSB) First Transmission Mode

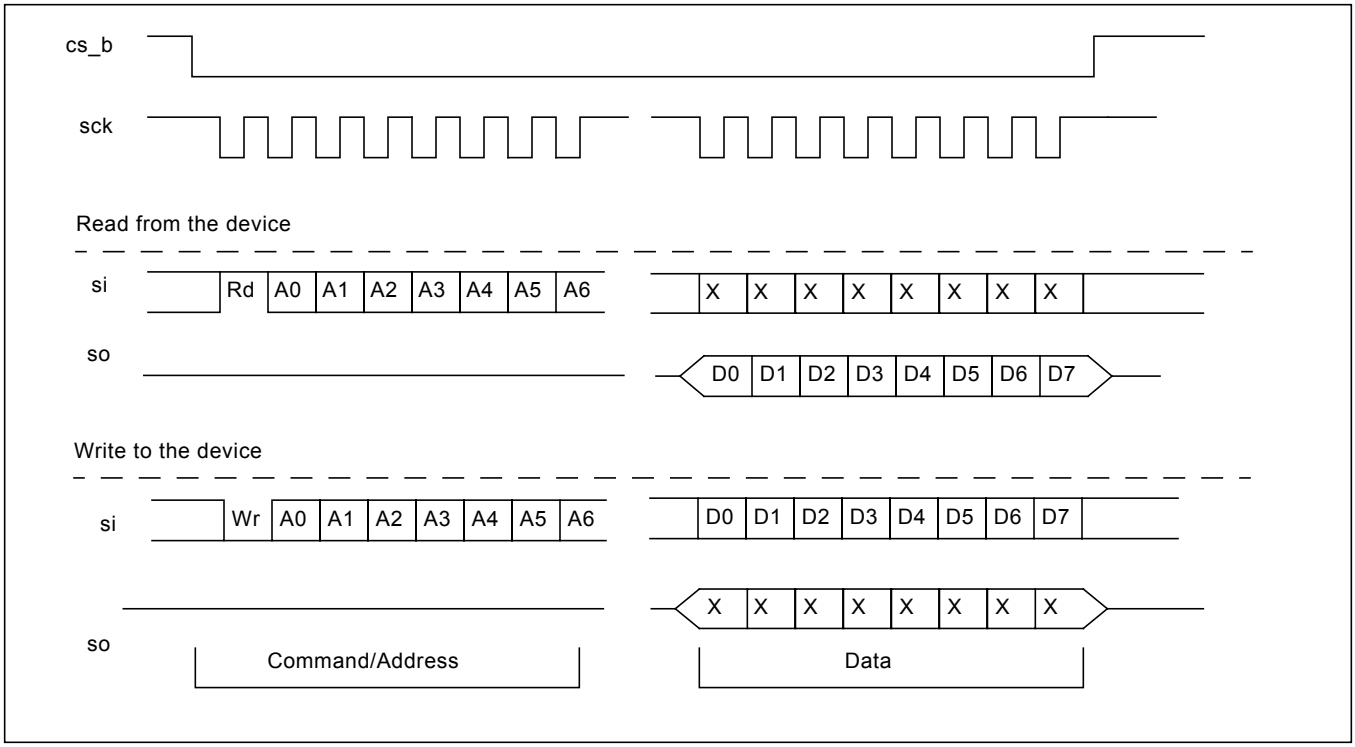


Figure 15 - Serial Peripheral Interface Functional Waveforms - LSB First Mode

6.1.2 Most Significant Bit (MSB) First Transmission Mode

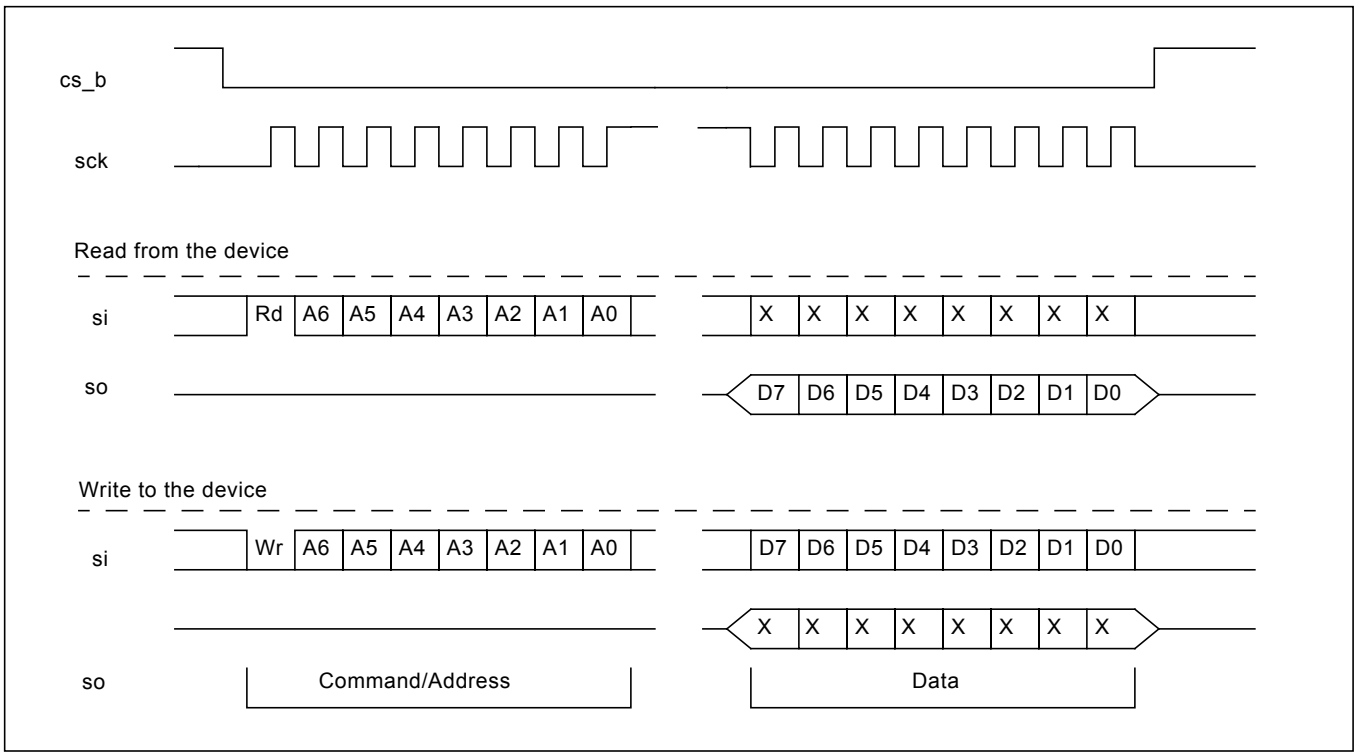


Figure 16 - Serial Peripheral Interface Functional Waveforms - MSB First Mode

6.1.3 SPI Burst Mode Operation

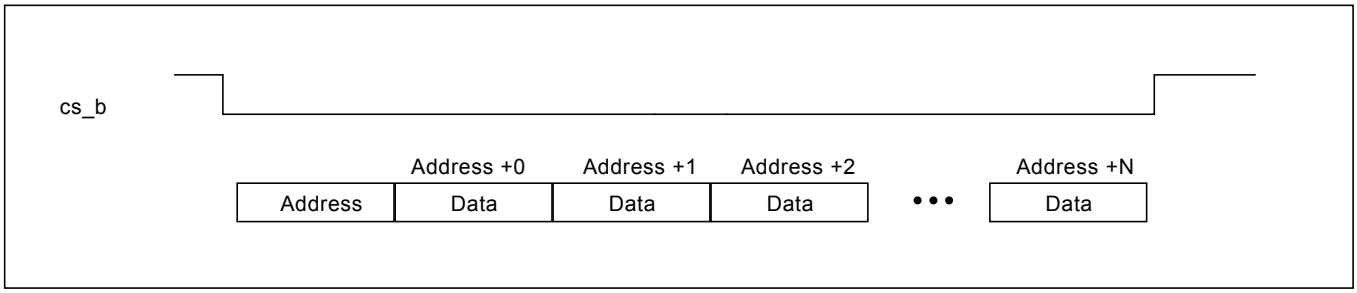


Figure 17 - Example of a Burst Mode Operation

6.1.4 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 18, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

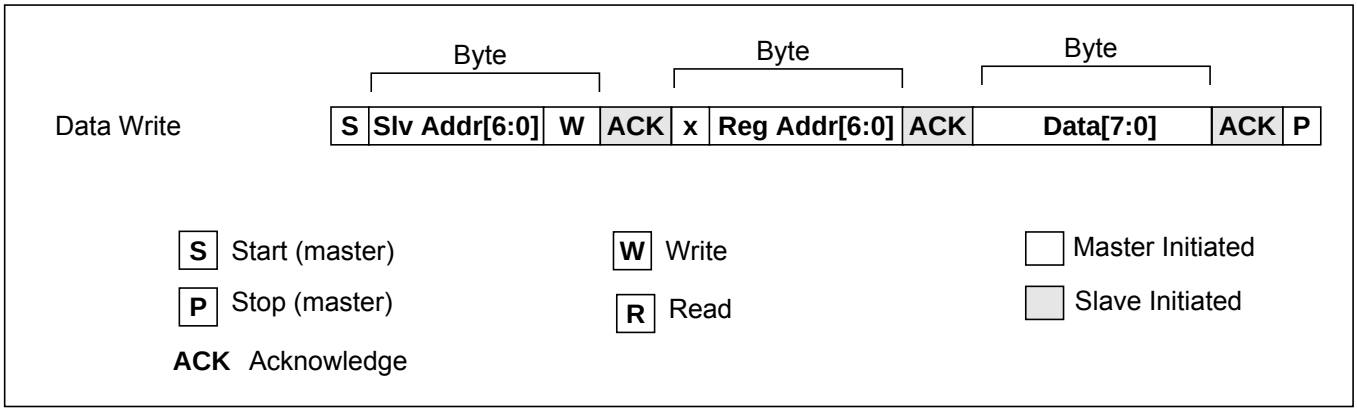


Figure 18 - I²C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 19.

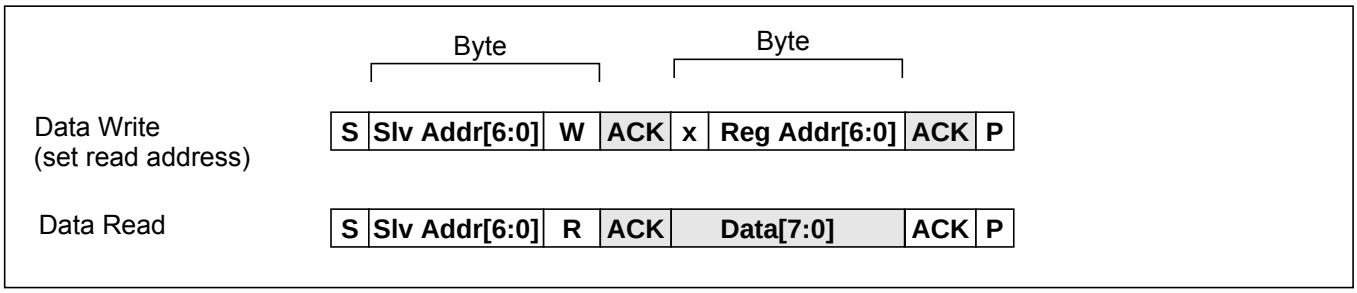


Figure 19 - I²C Data Read Protocol

The **7-bit device (slave) address** contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple similar devices to share the same I^{2}C bus. The address configuration is shown in Figure 20.

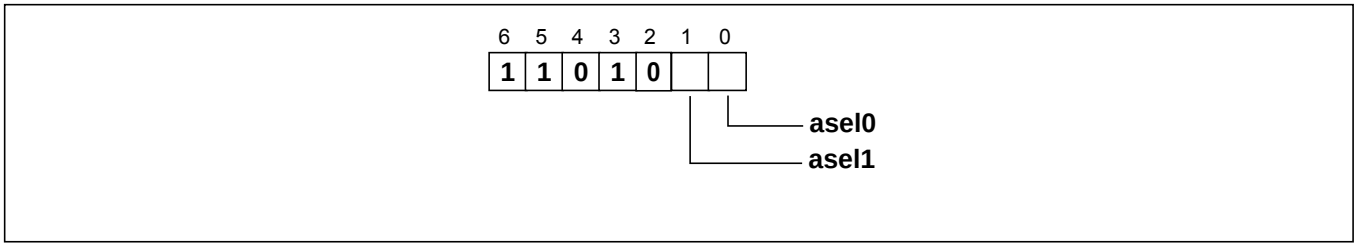


Figure 20 - I^{2}C 7-bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 21 (write) and Figure 22 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

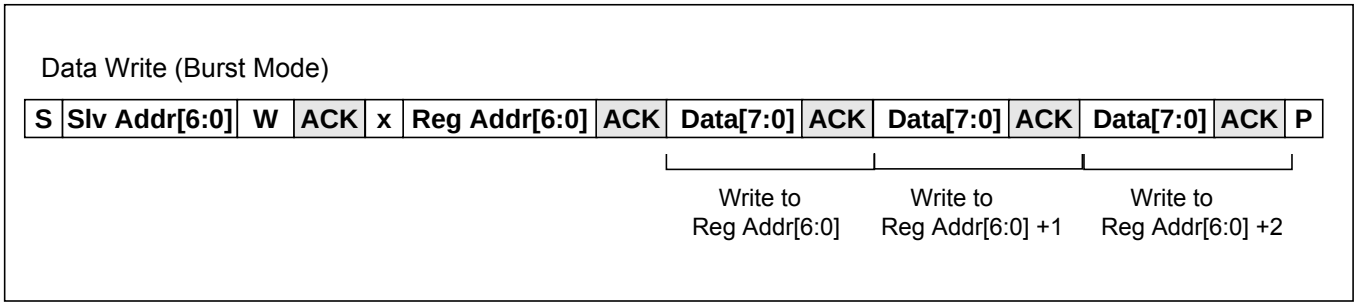


Figure 21 - I^{2}C Data Write Burst Mode

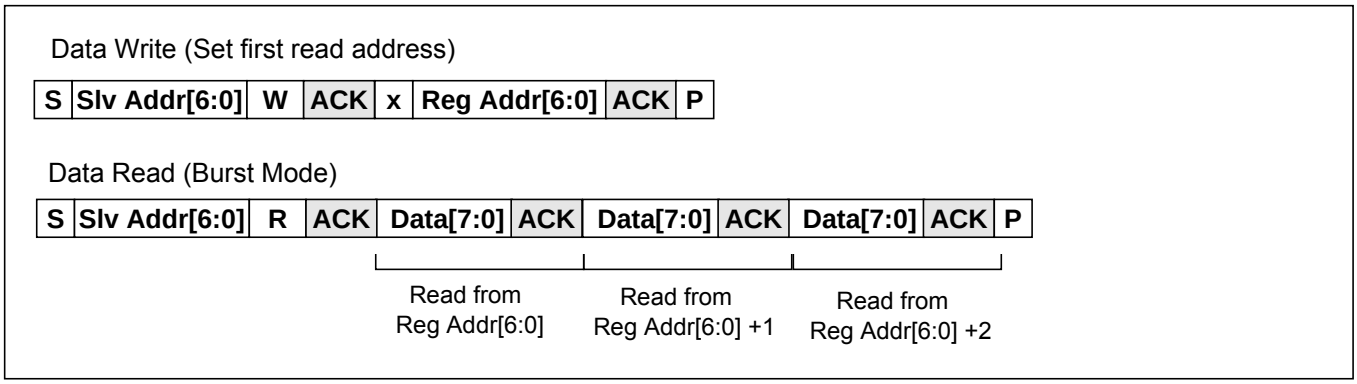


Figure 22 - I^{2}C Data Read Burst Mode

7.0 Register Map

The device is mainly controlled by accessing software registers through the serial interface (SPI or I^2C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

The simplest way to generate appropriate configuration for the device is to use the evaluation board GUI which can operate standalone (without the board). With GUI user can quickly set all required parameters and save the configuration to a text file.

Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order—they must follow big endian addressing scheme. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 23. When writing a multi-byte value, the value is latched when the LSB is written.

Example:
The programmable input reference M and N 16 bit values defining the M/N ratio is programmed using a 32-bit value which is spread over four 8-bit registers. The MSB is contained in address 0x14 and the LSB in 0x17. When reading or writing this multi-byte value, the MSB must be accessed first, followed by the middle bytes, and the LSB last.

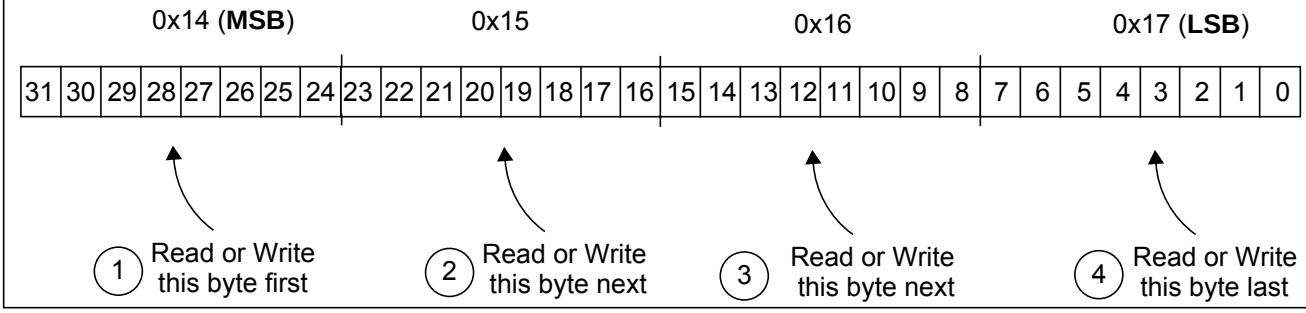


Figure 23 - Accessing Multi-byte Register Values

To assist in device setup, a configuration GUI is provided. The configuration GUI can directly configure the device evaluation board, but it also functions as a tool to provide details on how to configure different device registers.

Procedure for writing registers

For each of the following ZL30230 control registers, the user should implement the write procedure described below. Using this procedure to write other control registers is acceptable, but it is required for the registers listed below.

• Registers: 0x46, 0xB8and, 0xBA

-write 0x01 to Sticky_R_Lock Register at address 0x0D

-write to one or more ZL30230 control register(s)

-write 0x00 to Sticky_R_Lock Register at address 0x0D

Time between two write accesses to the same register

- User should wait at least 8 ms between two write accesses to the same register
- For page_register at address 0x7F, and Sticky_r_lock register at address 0x0D there is no waiting time required between two write accesses.

Reading from Sticky Read (StickyR) Registers

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-write 0x01 to StickyR Lock Register at address 0x0D

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x0D

-wait for 8 ms

-read the status register(s)

The following table provides a summary of the registers available for status updates and configuration of the device. Devices with a custom OTP configuration will power-up with the custom configuration values instead of the default values.

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Miscellaneous Registers				
0x00	id_reg	See Description	Chip ID and version identification	R
0x01	config_record_id [23:16]	0xFF	Configuration record identification, bits [23:16]	R
0x0E:0x0F	config_record_id [15:0]	0x0000	Configuration record identification, bits [15:0]	R
Output Synthesizer Configuration Registers				
0x46	reduced_diff_out_pwr	0xFF	Enables reduced power on high performance differential outputs	R/W
0x50:0x51	synth0_base_freq	0x9C40	Synthesizer 0 base frequency	R/W
0x52:0x53	synth0_freq_multiple	0x0798	Synthesizer 0 base frequency multiplication number	R/W
0x54:0x57	synth0_ratio_M_N	0x00010001	Specifies numerator Ms and denominator Ns for synthesizer 0 multiplication ratio Ms/Ns	R/W
0x58:0x59	synth1_base_freq	0x61A8	Synthesizer 1 base frequency	R/W
0x5A:0x5B	synth1_freq_multiple	0x0C35	Synthesizer 1 base frequency multiplication number	R/W
0x5C:0x5F	synth1_ratio_M_N	0x00010001	Specifies numerator Ms and denominator Ns for synthesizer 1 multiplication ratio Ms/Ns	R/W
0x60:0x61	synth2_base_freq	0x9C40	Synthesizer 2 base frequency	R/W
0x62:0x63	synth2_freq_multiple	0x0798	Synthesizer 2 base frequency multiplication number	R/W
0x64:0x67	synth2_ratio_M_N	0x00010001	Specifies numerator Ms and denominator Ns0 for synthesizer 2 multiplication ratio Ms/Ns	R/W
0x68:0x69	synth3_base_freq	0x9C40	Synthesizer 3 base frequency	R/W
0x6A:0x6B	synth3_freq_multiple	0x0798	Synthesizer 3 base frequency multiplication number	R/W

Table 5 - Register Map

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x6C:0x6F	synth3_ratio_M_N	0x00010001	Specifies numerator Ms and denominator Ns for synthesizer 3 multiplication ratio Ms/Ns	R/W
0x71	output_synthesizer_en	0x03	Output synthesizer enable	R/W
0x73:0x76	central_freq_offset	0x046AAAAB	Central frequency offset to compensate for oscillator inaccuracy	R/W
0x77	synth_1_0_filter_sel	0x00	Synthesizer 1 and 0 selection between internal and external filter	R/W
0x78	synth0_fine_phase_shift	0x00	Synthesizer 0 fine phase shift	R/W
0x79	synth1_fine_phase_shift	0x00	Synthesizer 1 fine phase shift	R/W
0x7A	synth2_fine_phase_shift	0x00	Synthesizer 2 fine phase shift	R/W
0x7B	synth3_fine_phase_shift	0x00	Synthesizer 3 fine phase shift	R/W
0x7F	page_register	0x00	Selects between pages 0 and 1	R/W
0x80:0x82	synth0_post_div_A	0x000002	Synthesizer 0 post divider A	R/W
0x83:0x85	synth0_post_div_B	0x000002	Synthesizer 0 post divider B	R/W
0x86:0x88	synth0_post_div_C	0x000040	Synthesizer 0 post divider C	R/W
0x89:0x8B	synth0_post_div_D	0x000040	Synthesizer 0 post divider D	R/W
0x8C,0x8E	synth1_post_div_A	0x000002	Synthesizer 1 post divider A	R/W
0x8F,0x91	synth1_post_div_B	0x000002	Synthesizer 1 post divider B	R/W
0x92,0x94	synth1_post_div_C	0x000032	Synthesizer 1 post divider C	R/W
0x95,0x97	synth1_post_div_D	0x000032	Synthesizer 1 post divider D	R/W
0x98,0x9A	synth2_post_div_A	0x000000	Synthesizer 2 post divider A	R/W
0x9B,0x9D	synth2_post_div_B	0x000000	Synthesizer 2 post divider B	R/W

Table 5 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x9E,0xA0	synth2_post_div_C	0x000000	Synthesizer 2 post divider C	R/W
0xA1,0xA3	synth2_post_div_D	0x000000	Synthesizer 2 post divider D	R/W
0xA4,0xA6	synth3_post_div_A	0x000000	Synthesizer 3 post divider A	R/W
0xA7,0xA9	synth3_post_div_B	0x000000	Synthesizer 3 post divider B	R/W
0xAA,0xAC	synth3_post_div_C	0x000000	Synthesizer 3 post divider C	R/W
0xAD,0xAF	synth3_post_div_D	0x000000	Synthesizer 3 post divider D	R/W
Output Reference Selection and Output Driver Control				
0xB0	hp_diff_en	0x00	High Performance differential output enable	R/W
0xB1	hp_cmos_en	0x00	Enables High Performance CMOS outputs hpoutclk[3:0]	R/W
0xB2	config_output_mode_7_4	0x00	Enables and controls configurable outputs outclk[7:4]	R/W
0xB3	config_output__mode_3_0	0x00	Enables and controls configurable outputs outclk[3:0]	R/W
0xB4	config_output_mux_7_4	0x00	Multiplexer selection for configurable outputs outclk[7:4]	R/W
0xB5	config_output_mux_3_0	0x00	Multiplexer selection for configurable outputs outclk[3:0]	R/W
0xB6	synth3_stop_clk	0x00	Stops output clocks for post dividers of Synthesis Engine 3 at either high or low logical level	R/W
0xB7	synth2_stop_clk	0x00	Stops output clocks for post dividers of Synthesis Engine 2 at either high or low logical level	R/W
0xB8	synth1_0_stop_clk	0x00	Stops output clocks for post dividers C and D of Synthesis Engine 0 and 1 at either high or low logical level	R/W
0xB9	sync_fail_flag_status	0x00	Indicates Synthesizers loss of lock	StickyR

Table 5 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xBA	clear_sync_fail_flag	0x00	Clears Synthesizers fail flag in register 0xB9	R/W
0xBF:0xC0	phase_shift_s0_postdiv_C	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 0, Post Divider C.	R/W
0xC1:0xC2	phase_shift_s0_postdiv_D	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 0, Post Divider D.	R/W
0XC3	xo_or_crystal_sel	0x00	Disables OSCo driver.	R/W
0xC6	Chip_Revision_2	0x03	Chip revision identification	R/W
0xC7:0xC8	phase_shift_s1_postdiv_C	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 1, Post Divider C.	R/W
0xC9:0xCA	phase_shift_s1_postdiv_D	0x0000	hpoutclk or configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 1, Post Divider D.	R/W
0xCB:0xCC	phase_shift_s2_postdiv_A	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider A.	R/W
0xCD:0xCE	phase_shift_s2_postdiv_B	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider B.	R/W
0xCF:0xD0	phase_shift_s2_postdiv_C	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider C.	R/W

Table 5 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xD1:0xD2	phase_shift_s2_postdiv_D	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 2, Post Divider D.	R/W
0xD3:0xD4	phase_shift_s3_postdiv_A	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider A.	R/W
0xD5:0xD6	phase_shift_s3_postdiv_B	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider B.	R/W
0xD7:0xD8	phase_shift_s3_postdiv_C	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider C.	R/W
0xD9:0xDA	phase_shift_s3_postdiv_D	0x0000	Configurable output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock steps for all clocks coming from Synthesizer 3, Post Divider D.	R/W
0xDB	config_output_voltage	0x00	Configurable output voltage level selection	R/W
0xDC	config_output_slew_rate	0x00	Configurable output slew rate control	R/W
0xE0	gpio_function_pin0	0x00	GPIO control or status select	R/W
0xE1	gpio_function_pin1	0x00	GPIO control or status select	R/W
0xE2	gpio_function_pin2	0x60	GPIO control or status select	R/W
0xE3	gpio_function_pin3	0x00	GPIO control or status select	R/W
0xE4	gpio_function_pin4	0x00	GPIO control or status select	R/W
0xE5	gpio_function_pin5	0x00	GPIO control or status select	R/W
0xE6	gpio_function_pin6	0x00	GPIO control or status select	R/W
0xE7	gpio_function_pin7	0x00	GPIO control or status select	R/W
0xE8	gpio_function_pin8	0x00	GPIO control or status select	R/W
0xE9	gpio_function_pin9	0x00	GPIO control or status select	R/W

Table 5 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xEA	gpio_function_pin10	0x00	GPIO control or status select	R/W
0xEB	gpio_function_pi11	0x00	GPIO control or status select	R/W
0xF7	spurs_suppression	0x00	Used for spurs suppression	R/W

Table 5 - Register Map (continued)

8.0 Detailed Register Map

Register_Address: **0x00** Register Name: **id_reg** Default Value:**See Description** Type: R/W		
Bit Field	**Function Name**	**Description**
4:0	chip_id	Chip Identification = 0b00011
6:5	chip_revision	Chip revision number = 0b00 Note:also see Chip_revision_2 register description at Register _Address: 0xC6 for full chip revision information
7	ready_indication	After reset this bit goes high when device is ready. This signals that user can start to program/configure the device. It can take up to 50 ms for this bit to go high after the reset. This bit should not be polled until 40ms after reset.

Register_Address: **0x01** Register Name:: **config_record_id [23:16]** Default Value:**0xFF** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	config_record_id	Bits [23:16] of the config_record_id. See application note ZLAN-301 to understand how to translate the config_record_id into an alpha-numeric CCID (Custom Configuration Identification). Valid config_record_id values are 0x000000 to 0x0E1780 and 0xFF0000. Devices with a factory default reset configuration report a config_record_id value of 0xFF0000.

Register_Address: **0x0D** Register Name: **sticky_r_lock** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	sticky_r_lock	This register is used when accessing StickyR status registers. Writing 0x01 to this register locks the status register from being updated by internal logic. Writing 0x00 to this register enables internal updates of StickyR status registers Please refer to **Reading from Sticky Read (StickyR) registers and Procedure for writing registers** procedure at the beginning of 7.0, “Register Map“ section.

Register_Address: **0x0E:0x0F**
Register Name:: **config_record_id [15:0]**
Default Value:**0x0000**
Type: R/W

Bit Field	Function Name	Description
15:0	config_record_id	Bits [15:0] of the config_record_id. See application note ZLAN-301 to understand how to translate the config_record_id into an alpha-numeric CCID (Custom Configuration Identification). Valid config_record_id values are 0x000000 to 0x0E1780 and 0xFF0000. Devices with a factory default reset configuration report a config_record_id value of 0xFF0000.

Register_Address: **0x46**
Register Name: **reduced_diff_out_pw**
Default Value: **0xFF**
Type: R/W

Bit Field	Function Name	Description
0	hpout0_reduced_pwr	When this bit is set to high, it will enable reduced power mode for HPDIFF0_P and HPDIFF0_N outputs. When low, the outputs are in full power mode.
1	hpout1_reduced_pwr	Same description as above but for HPDIFF1 output.
2	hpout2_reduced_pwr	Same description as above but for HPDIFF2 output.
3	hpout3_reduced_pwr	Same description as above but for HPDIFF3 output.
4	hpout4_reduced_pwr	Same description as above but for HPDIFF4 output.
5	hpout5_reduced_pwr	Same description as above but for HPDIFF5 output.
6	hpout6_reduced_pwr	Same description as above but for HPDIFF6 output.
7	hpout7_reduced_pwr	Same description as above but for HPDIFF7 output.

Register_Address: **0x50:0x51**
Register Name: **synth0_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth0_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer0 base frequency Bs in Hz. Values for Br that can be programmed: 0x03E8 for 1 kHz, 0x07D0 for 2 kHz, 0x1388 for 5 kHz, 0x186A for 6.25 kHz, 0x1F40 for 8 kHz, 0x2710 for 10 kHz, 0x30D4 for 12.5 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note:** Other Bs rates can be supported, please contact the CMPG application support team if another specific Bs rate is required

Register_Address: **0x52:0x53**
Register Name: **synth0_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth0_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer0 base frequency multiplication number. For regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 8 has to equal the synthesizer frequency in Hz. **Note 1:** synthesizer frequency has to programmed to be between 1 GHz and 1.5 GHz, so: Bs x Ks x 16 x Ms / Ns has to be between 1 000 000 000 and 1 500 000 000. Examples of some references frequencies and appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency — Base frequency Bs — Base frequency multiple Ks 1.048576 GHz — 8 kHz (0x1F40) — 8192 (0x2000) 1.24416 GHz — 40 kHz (0x9C40) — 1944 (0x0798) 1.25 GHz — 25 kHz (0x61A8) — 3125 (0x0C35) **Note 2:** Synthesizer 0 and 1 can be set to generate identical frequencies if that frequency is between 1.1 GHz and 1.5 GHz. For frequencies between 1.0 GHz and 1.1 GHz Synthesizers 0 and 1 should not be set to generate the same frequency. In this case user should try to set one Synthesizer to lower range (1.0 GHz to 1.25 GHz) and the other to the higher range (1.25 GHz to 1.5 GHz) and then use different values for output dividers to get the same frequency at the output. This method can be used for all output frequencies except for output frequencies in 500 MHz to 550 MHz range. Please contact your local Field Applications Engineer for recommendations if output frequencies sourced from both high performance synthesizer need to be the same and in 500 MHz to 550 MHz range.

Register_Address: **0x54:0x57**
Register Name: **synth0_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth0_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer0 FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to 0x0001 (default values) Examples of some synthesizer FEC frequencies and appropriate values that can be programmed for the Bs, Ks, Ms and Ns registers to get those FEC frequencies: **a) OC-192 mode, standard EFEC for long reach:** Desired frequency: 155.52 MHz x 255 / 237 Synth frequency: 1.24416 GHz x 255/237 Base frequency Bs: 40 kHz (0x9C40) Base freq. multiplier Ks: 1944 (0x0798) FEC ratio numerator Ms: 255 (0x00FF) FEC ratio denominator Ns: 237 (0x00ED) Post div PA: 8 **b) Long reach 10GE mode, double rate conversion:** Desired frequency: 156.25MHz x 66/64 x 255/238 Synth frequency: 1.25GHz x 66/64 x 255/238 Base frequency Bs: 25 kHz (0x061A8) Base freq. multiplier Ks: 3125 (0x0C35) FEC ratio numerator Ms: 66x255 (0x41BE) FEC ratio denominator Ns: 64x238 (0x3B80) Post div PA: 8
31:16	synth0_ratio_numer_Ms	

Register_Address: **0x58:0x59**
Register Name: **synth1_base_freq**
Default Value: **0x61A8**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth1_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer1 base frequency Bs in Hz. Values for Br that can be programmed: 0x03E8 for 1 kHz, 0x07D0 for 2 kHz, 0x1388 for 5 kHz, 0x186A for 6.25 kHz, 0x1F40 for 8 kHz, 0x2710 for 10 kHz, 0x30D4 for 12.5 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note:** Other Bs rates can be supported, please contact the CMPG application support team if another specific Bs rate is required.

Register_Address: **0x5A:0x5B**
Register Name: **synth1_freq_multiple**
Default Value: **0x0C35**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth1_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer0 base frequency multiplication number. For regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 has to equal the synthesizer frequency in Hz. **Note 1:** synthesizer frequency has to be between 1 GHz and 1.5 GHz, so: Bs x Ks x 16 x Ms / Ns has to be between 1 000 000 000 and 1 500 000 000. Examples of some synthesizer frequencies and appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency — Base frequency Bs — Base frequency multiple Ks 1.048576 GHz — 8 kHz (0x1F40) — 8192 (0x2000) 1.24416 GHz — 40 kHz (0x9C40) — 1944 (0x0798) 1.25 GHz — 25 kHz (0x61A8) — 3125 (0x0C35) **Note 2:** Synthesizer 0 and 1 can be set to generate identical frequencies if that frequency is between 1.1 GHz and 1.5 GHz. For frequencies between 1.0 GHz and 1.1 GHz Synthesizers 0 and 1 should not be set to generate the same frequency. In this case user should try to set one Synthesizer to lower range (1.0 GHz to 1.25 GHz) and the other to the higher range (1.25 GHz to 1.5 GHz) and then use different values for output dividers to get the same frequency at the output. This method can be used for all output frequencies except for output frequencies in 500 MHz to 550 MHz range. Please contact your local Field Applications Engineer for recommendations if output frequencies sourced from both high performance synthesizer need to be the same and in 500 MHz to 550 MHz range.

Register_Address: **0x5C:0x5F**
Register Name: **synth1_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth1_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer1 FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to 0x0001 (default values) Examples of some synthesizer FEC frequencies and appropriate values that can be programmed for the Bs, Ks, Ms and Ns registers to get those FEC frequencies: **a) OC-192 mode, standard EFEC for long reach:** Desired frequency: 155.52 MHz x 255 / 237 Synth frequency: 1.24416 GHz x 255/237 Base frequency Bs: 40 kHz (0x9C40) Base freq. multiplier Ks: 1944 (0x0798) FEC ratio numerator Ms: 255 (0x00FF) FEC ratio denominator Ns: 237 (0x00ED) Post div PA: 8 **b) Long reach 10GE mode, double rate conversion:** Desired frequency: 156.25MHz x 66/64 x 255/238 Synth frequency: 1.25GHz x 66/64 x 255/238 Base frequency Bs: 25 kHz (0x061A8)) Base freq. multiplier Ks: 3125 (0x0C35) FEC ratio numerator Ms: 66x255 (0x41BE) FEC ratio denominator Ns: 64x238 (0x3B80) Post div PA: 8
31:16	synth1_ratio_numer_Ms	

Register_Address: **0x60:0x61**
Register Name: **synth2_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth2_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer2 base frequency Bs in Hz.Values for Br that can be programmed: 0x03E8 for 1 kHz, 0x07D0 for 2 kHz, 0x1388 for 5 kHz, 0x186A for 6.25 kHz, 0x1F40 for 8 kHz, 0x2710 for 10 kHz, 0x30D4 for 12.5 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note:** Other Bs rates can be supported, please contact the CMPG application support team if another specific Bs rate is required.

Register_Address: **0x62:0x63**
Register Name: **synth2_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth2_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer2 base frequency multiplication number. For regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 8 has to equal the synthesizer frequency in Hz. Important limitation: synthesizer frequency has to programmed to be between 500 MHz and 750 MHz, so: Bs x Ks x 8 x Ms / Ns has to be between 500 000 000 and 750 000 000. Examples of some references frequencies and appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency — Base frequency Bs — Base frequency multiple Ks 524.288 MHz — 8 kHz (0x1F40) — 8192 (0x2000) 622.08 MHz — 40 kHz (0x9C40) — 1944 (0x0798) 625.MHz — 25 kHz (0x61A8) — 3125 (0x0C35)

Register_Address: **0x64:0x67**
Register Name: **synth2_fec_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth2_fec_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer2 FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 8 x Ms / Ns For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to 0x0001 (default values) Examples of some synthesizer FEC frequencies and appropriate values that can be programmed for the Bs, Ks, Ms and Ns registers to get those FEC frequencies: **a) OC-192 mode, standard EFEC for long reach:** Desired frequency: 155.52 MHz x 255 / 237 Synth frequency: 622.08MHz x 255/237 Base frequency Bs: 40 kHz (0x9C40) Base freq. multiplier Ks: 1944 (0x0798) FEC ratio numerator Ms: 255 (0x00FF) FEC ratio denominator Ns: 237 (0x00ED) Post div PA: 4 **b) Long reach 10GE mode, double rate conversion:** Desired frequency: 156.25MHz x 66/64 x 255/238 Synth frequency: 625MHz x 66/64 x 255/238 Base frequency Bs: 25 kHz (0x061A8)) Base freq. multiplier Ks: 3125 (0x0C35) FEC ratio numerator Ms: 66x255 (0x41BE) FEC ratio denominator Ns: 64x238 (0x3B80) Post div PA: 4
31:16	synth2_fec_ratio_numer_Ms	

Register_Address: **0x68:0x69**
Register Name: **synth3_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth3_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer3 base frequency Bs in Hz.Values for Br that can be programmed: 0x03E8 for 1 kHz, 0x07D0 for 2 kHz, 0x1388 for 5 kHz, 0x186A for 6.25 kHz, 0x1F40 for 8 kHz, 0x2710 for 10 kHz, 0x30D4 for 12.5 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note:** Other Bs rates can be supported, please contact the CMPG application support team if another specific Bs rate is required.

Register_Address: **0x6A:0x6B**
Register Name: **synth3_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth3_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer3 base frequency multiplication number. For regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 8 has to equal the synthesizer frequency in Hz. Important limitation: synthesizer frequency has to programmed to be between 500 MHz and 750 MHz, so: Bs x Ks x 8 x Ms / Ns has to be between 500 000 000 and 750 000 000. Examples of some references frequencies and appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency — Base frequency Bs — Base frequency multiple Ks 524.288 MHz — 8 kHz (0x1F40) — 8192 (0x2000) 622.08 MHz — 40 kHz (0x9C40) — 1944 (0x0798) 625 MHz — 25 kHz (0x61A8) — 3125 (0x0C35)

Register_Address: **0x6C:0x6F**
Register Name: **synth3_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth3_fec_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer3 FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 8 x Ms / Ns For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to 0x0001 (default values) Examples of some synthesizer FEC frequencies and appropriate values that can be programmed for the Bs, Ks, Ms and Ns registers to get those FEC frequencies: **a) OC-192 mode, standard EFEC for long reach:** Desired frequency: 155.52 MHz x 255 / 237 Synth frequency: 622.08MHz x 255/237 Base frequency Bs: 40 kHz (0x9C40) Base freq. multiplier Ks: 1944 (0x0798) FEC ratio numerator Ms: 255 (0x00FF) FEC ratio denominator Ns: 237 (0x00ED) Post div PA: 4 **b) Long reach 10GE mode, double rate conversion:** Desired frequency: 156.25MHz x 66/64 x 255/238 Synth frequency: 625MHz x 66/64 x 255/238 Base frequency Bs: 25 kHz (0x061A8)) Base freq. multiplier Ks: 3125 (0x0C35) FEC ratio numerator Ms: 66x255 (0x41BE) FEC ratio denominator Ns: 64x238 (0x3B80) Post div PA: 4
31:16	synth3_fec_ratio_numer_Ms	

Register_Address: **0x71**
Register Name: **output_synth_en**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
3:0	synth_en	Enables output of Synthesizers 0 to 3 xxx1: enables synth0 output xx1x: enables synth1 output x1xx: enables synth2 output 1xxx: enables synth3 output
7:4	reserved	reserved

Register_Address: **0x73:0x76**
Register Name: **central_freq_offset**
Default Value: **0x046AAAAB**
Type:**R/W**

Bit Field	Function Name	Description
31:0	central_freq_offset	2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy, or make the device look like Numerically Controlled Oscillator (NCO). This register controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), value to be programmed in this register is calculated as per the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e., 25 MHz) Generally, when the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1): if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02), X= (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A Example 2): if oscillator inaccuracy is +2% (f_osc = 25.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = 0.02), X= (1/(1+ 0.02))*2^32 = (1/1.02)*2^32 = 4210752251 = 0xFAFAFAFB When NCO behavior is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for particular VCO fout - output frequency **Note 1:** Nominal frequency for central frequency offset calculation is 25 MHz although master clock frequency is required to be 24.576 MHz. Because of this default value in this register is 0x046AAAAB. **Note 2:** Central Frequency Offset should not exceed +/-5% off nominal.

Register_Address: **0x77**
Register Name: **synth1_0_filter_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	synth0_filter_select	Selects filter used by Synthesizer 0 0: external filter 1: internal filter
1	synth1_filter_select	Selects filter used by Synthesizer 1 0: external filter 1: internal filter
7:2	reserved	reserved

Register_Address: **0x78**
Register Name: **synth0_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	syn0_fine_phase_shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of Synth0_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 0 (including all four post dividers)

Register_Address: **0x79**
Register Name: **synth1_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	syn1_fine_phase_shift	Unsigned binary value of these bits represent Synth1 fine phase shift (advancement) in steps of Synth1_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 1 (including all four post dividers)

Register_Address: **0x7A**
Register Name: **synth2_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	syn2_fine_phase_shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of Synth2_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 2 (including all four post dividers)

Register_Address: **0x7B**
Register Name: **synth3_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	syn3_fine_phase_shift	Unsigned binary value of these bits represent Synth3 fine phase shift (advancement) in steps of Synth3_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 3 (including all four post dividers)

Register_Address: **0x7F**
Register Name: **page_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	page_select	This register is used to toggle memory access between page 0 (addresses 0x00 to 0x7E) and page 1 (addresses 0x80 to 0xFF). This is required because SPI and I2C ports have only seven address bits and the device memory space is eight bit wide. 0: selects addresses 0x00 to 0x7E 1: selects addresses 0x80 to 0xFB
7:1	reserved	reserved

Register_Address: **0x80:0x82**
Register Name: **synth0_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
22:0	synth0_post_div_A	Unsigned binary value represents Synthesizer0 Post Divider value P0A. The Synthesizer0 frequency is divided by the P0A value before being fed to the selected output pins
23	reserved	This bit **must** be set to 0

Register_Address: **0x83:0x85**
Register Name: **synth0_post_div_B**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
22:0	synth0_post_div_B	Unsigned binary value represents Synthesizer0 Post Divider value P0B. The Synthesizer0 frequency is divided by the P0B value before being fed to the selected output pins
23	reserved	This bit **must** be set to 0

Register_Address: **0x86:0x88**
Register Name: **synth0_post_div_C**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer0 Post Divider value P0C). The Synthesizer0 VCO frequency is divided by the P0C value to get desired output clock frequency on selected output pins. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P0C is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P0C is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and P0C to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P0C values greater than or equal to 41 (43, 45 ...) the duty-cycle will be within 45% to 55%. For even P0C values duty-cycle is always within 45% to 55%.
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 0 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 0 postdivider A) 01: clock 1 (Synth 0 postdivider B) 10: reserved 11: clock 3 (Synth 0 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock

Register_Address: **0x86:0x88**
Register Name: **synth0_post_div_C**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock. **Note:** Polarity is reversed if the frame pulse is selected by registers 0xB5 to appear on configurable output pins.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x89:0x8B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer0 Post Divider value P0D). The Synthesizer0 VCO frequency is divided by the P0D value to get desired output clock frequency on selected output pins. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P0D is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P0D is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and P0D to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P0D values greater than or equal to 41 (43, 45 ...) the duty-cycle will be within 45% to 55%. For even P0D values duty-cycle is always within 45% to 55%.
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 0 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 0 postdivider A) 01: clock 1 (Synth 0 postdivider B) 10: clock 2 (Synth 0 postdivider C) 11: reserved When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock

Register_Address: **0x89:0x8B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock. **Note:** Polarity is reversed if the frame pulse is selected by registers 0xB5 to appear on configurable output pins.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x8C:0x8E**
Register Name: **synth1_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
22:0	synth1_post_div_A	Unsigned binary value represents Synthesizer1 Post Divider value P1A. The Synthesizer1 frequency is divided by the P1A value before being fed to the selected output pins
23	reserved	This bit **must** be set to 0

Register_Address: **0x8F:0x91**
Register Name: **synth1_post_div_B**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
22:0	synth1_post_div_B	Unsigned binary value represents Synthesizer1 Post Divider value P1B. The Synthesizer1 frequency is divided by the P1B value before being fed to the selected output pins
23	reserved	This bit **must** be set to 0

Register_Address: **0x92:0x94**
Register Name: **synth1_post_div_C**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer1 Post Divider value P1C). The Synthesizer1 VCO frequency is divided by the P1C value to get desired output clock frequency on selected output pins. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P1C is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P1C is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and P1C to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P1C values greater than or equal to 41 (43, 45 ...) the duty-cycle will be within 45% to 55%. For even P1C values duty-cycle is always within 45% to 55%.
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 1 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 1 postdivider A) 01: clock 1 (Synth 1 postdivider B) 10: reserved 11: clock 3 (Synth 1 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock

Register_Address: **0x92:0x94**
Register Name: **synth1_post_div_C**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock. **Note:** Polarity is reversed if the frame pulse is selected by registers 0xB4 to appear on configurable output pins.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x95:0x97**
Register Name: **synth1_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer1 Post Divider value P1D). The Synthesizer1 VCO frequency is divided by the P1D value to get desired output clock frequency on selected output pins. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value P1D is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the P1D is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and P1D to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd P1D values greater than or equal to 41 (43, 45 ...) the duty-cycle will be within 45% to 55%. For even P1D values duty-cycle is always within 45% to 55%.
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 1 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 1 postdivider A) 01: clock 1 (Synth 1 postdivider B) 10: clock 2 (Synth 1 postdivider C) 11: reserved When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock

Register_Address: **0x95:0x97**
Register Name: **synth1_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock. **Note:** Polarity is reversed if the frame pulse is selected by registers 0xB4 to appear on configurable output pins.
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x98:0x9A**
Register Name: **synth2_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer2 Post Divider value P2A). The Synthesizer2 VCO frequency is divided by the P2A value to get desired output clock frequency on selected output pins.
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 2 (frame pulse width is equal to the related clock period): 00: reserved 01: clock 1 (Synth 2 postdivider B) 10: clock 2 (Synth 2 postdivider C) 11: clock 3 (Synth 2 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0x98:0x9A**
Register Name: **synth2_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x9B:0x9D**
Register Name: **synth2_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer2 Post Divider value P2B). The Synthesizer2 VCO frequency is divided by the P2B value to get desired output clock frequency on selected output pins.

Register_Address: **0x9B:0x9D**
Register Name: **synth2_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 2 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 2 postdivider A) 01: reserved 10: clock 2 (Synth 2 postdivider C) 11: clock 3 (Synth 2 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0x9B:0x9D**
Register Name: **synth2_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0x9E:0xA0**
Register Name: **synth2_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer2 Post Divider value P2C). The Synthesizer2 VCO frequency is divided by the P2C value to get desired output clock frequency on selected output pins.

Register_Address: **0x9E:0xA0**
Register Name: **synth2_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 2 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 2 postdivider A) 01: clock 1 (Synth 2 postdivider B) 10: reserved 11: clock 3 (Synth 2 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. Note: It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0x9E:0xA0**
Register Name: **synth2_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) Note: Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xA1:0xA3**
Register Name: **synth2_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer2 Post Divider value P2D). The Synthesizer2 VCO frequency is divided by the P2D value to get desired output clock frequency on selected output pins.

Register_Address: **0xA1:0xA3**
Register Name: **synth2_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 2 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 2 postdivider A) 01: clock 1 (Synth 2 postdivider B) 10: clock 2 (Synth 2 postdivider C) 11: reserved When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0xA1:0xA3**
Register Name: **synth2_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) Note: Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xA4:0xA6**
Register Name: **synth3_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer3 Post Divider value P3A). The Synthesizer3 VCO frequency is divided by the P3A value to get desired output clock frequency on selected output pins.

Register_Address: **0xA4:0xA6**
Register Name: **synth3_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 3 (frame pulse width is equal to the related clock period): 00: reserved 01: clock 1 (Synth 3 postdivider B) 10: clock 2 (Synth 3 postdivider C) 11: clock 3 (Synth 3 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0xA4:0xA6**
Register Name: **synth3_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xA7:0xA9**
Register Name: **synth3_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer3 Post Divider value P3B). The Synthesizer3 VCO frequency is divided by the P3B value to get desired output clock frequency on selected output pins.

Register_Address: **0xA7:0xA9**
Register Name: **synth3_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 3 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 3 postdivider A) 01: reserved 10: clock 2 (Synth 3 postdivider C) 11: clock 3 (Synth 3 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. Note: It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0xA7:0xA9**
Register Name: **synth3_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xAA:0xAC**
Register Name: **synth3_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer3 Post Divider value P3C). The Synthesizer3 VCO frequency is divided by the P3C value to get desired output clock frequency on selected output pins.

Register_Address: **0xAA:0xAC**
Register Name: **synth3_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 3 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 3 postdivider A) 01: clock 1 (Synth 3 postdivider B) 10: reserved 11: clock 3 (Synth 3 postdivider D) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0xAA:0xAC**
Register Name: **synth3_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xAD:0xAF**
Register Name: **synth3_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	frm_pulse_period_or_div	When bits 23:20 of this register are programmed to '1111', binary value of these bits represent number of periods of the selected related clock in between two frame pulses When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock (Synthesizer3 Post Divider value P3D). The Synthesizer3 VCO frequency is divided by the P3D value to get desired output clock frequency on selected output pins.

Register_Address: **0xAD:0xAF**
Register Name: **synth3_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
17:16	frm_pulse_clk_sel_or_div	When bits 23:20 of this register are programmed to '1111', these bits select related clock (postdivider) within the same synthesizer 3 (frame pulse width is equal to the related clock period): 00: clock 0 (Synth 3 postdivider A) 01: clock 1 (Synth 3 postdivider B) 10: clock 2 (Synth 3 postdivider C) 11: reserved When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with other bits of this register creates postdivider ratio for the output clock. **Note:** It is forbidden for frame pulse to select 'itself' as its related clock
18	frm_pulse_polar_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse polarity: 0: regular (non-inverse) polarity 1: inverse polarity When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock
19	frm_pulse_type_or_div	When bits 23:20 of this register are programmed to '1111', this bit represents frame pulse type: 0: ST-BUS type frame pulse (frame boundary straddles in the middle of the frame pulse) 1: GCI Bus type frame pulse (frame boundary defined by the edge of the frame pulse) When bits 23:20 of this register are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of this bit combined with other bits of this register creates postdivider ratio for the output clock

Register_Address: **0xAD:0xAF**
Register Name: **synth3_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	frm_pulse_or_div	When these bits are programmed to '1111', the appropriate output clock is selected to have a 'frame pulse' shape. Details about the frame pulse type, polarity and frequency are specified in bits 19:0 of this register. When these bits are programmed to any other value, the appropriate output clock is selected to have a 'normal' 50% duty cycle clock, and binary value of these bits combined with bits 19:0 of this register creates postdivider ratio for the output clock (i.e. division ratio between appropriate VCO frequency and the desired output clock frequency) **Note:** Maximum division ratio for 'normal' clock is 0xEFFFFF = 15728639.

Register_Address: **0xB0**
Register Name: **hp_diff_en**
Default Value: **0x55**
Type:**R/W**

Bit Field	Function Name	Description
7:0	hp_diff_en	Set high to enable corresponding high performance differential output. Set low to tristate the corresponding output. xxxxxxx1: enables hpdiff0_p/n xxxxxx1x: enables hpdiff1_p/n xxxxx1xx: enables hpdiff2_p/n xxxx1xxx: enables hpdiff3_p/n xxx1xxxx: enables hpdiff4_p/n xx1xxxxx: enables hpdiff5_p/n x1xxxxxx: enables hpdiff6_p/n 1xxxxxxx: enables hpdiff7_p/n

Register_Address: **0xB1**
Register Name: **hp_cmos_en**
Default Value: **0x0F**
Type:**R/W**

Bit Field	Function Name	Description
3:0	hp_cmos_en	Set high to enable corresponding high performance output. Set low to tristate the corresponding output. xxx1: enables hpout0 xx1x: enables hpout1 x1xx: enables hpout2 1xxx: enables hpout3
7:4	reserved	reserved

Register_Address: **0xB2**
Register Name: **config_output_mode_7_4**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
2:0	config_output_mode_5_4	These bits are used to enable outputs, and to select the mode of operation for configurable outputs 4 and 5 000: disable outputs 001: enable outclk4 in CMOS mode 010: enable outclk5 in CMOS mode 011: enable outclk4 and outclk5 in CMOS mode 100: enable outclk4 and outclk5 in complementary CMOS mode (outclk5 is inverted outclk4) 101: enable HCSL differential outputs 110: enable LVDS differential outputs 111: enable PECL differential outputs
3	reserved	reserved
6:4	config_output_mode_7_6	description same as for config_output_mode_5_4 above
7	reserved	reserved

Register_Address: **0xB3**
Register Name: **config_output_mode_3_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
2:0	config_output_mode_1_0	These bits are used to enable outputs, and to select the mode of operation for configurable outputs 0 and 1 000: disable outputs 001: enable outclk0 in CMOS mode 010: enable outclk1 in CMOS mode 011: enable outclk0 and outclk1 in CMOS mode 100: enable outclk0 and outclk1 in complementary CMOS mode (outclk1 is inverted outclk0) 101: enable HCSL differential outputs 110: enable LVDS differential outputs 111: enable PECL differential outputs
3	reserved	reserved
6:4	config_output_mode_3_2	description same as for config_output_mode_1_0 above
7	reserved	reserved

Register_Address: **0xB4**
Register Name: **config_output_mux_7_4**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	config_mux_output_4	These bits determine which clock will be selected to appear on outclk4 output in both, single ended and differential mode. 00: S3_A (Synthesis Engine 3, Divider A) 01: S1_C 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB4**
Register Name: **config_output_mux_7_4**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
3:2	config_mux_output_5	These bits determine which clock will be selected to appear on outclk5 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk4 and outclk5, these bits are ignored and outclk5 will have inverted version of outclk4 output clock. 00: S3_C (Synthesis Engine 3, Divider C) 01: S1_D 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
5:4	config_mux_output_6	These bits determine which clock will be selected to appear on outclk6 output in both, single ended and differential mode. 00: S3_A (Synthesis Engine 3, Divider A) 01: S1_C 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
7:6	config_mux_output_7	these bits determine which clock will be selected to appear on outclk7 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk6 and outclk7, these bits are ignored and outclk7 will have inverted version of outclk6 output clock. 00: S3_D (Synthesis Engine 3, Divider D) 01: S1_D 10 and 11: reserved **Note:** Synthesizer 3 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 1 (S1) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB5**
Register Name: **config_output_mux_3_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	config_mux_output_0	These bits determine which clock will be selected to appear on outclk0 output in both, single ended and differential mode. 00: S2_A (Synthesis Engine 2, Divider A) 01: S0_C 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
3:2	config_mux_output_1	These bits determine which clock will be selected to appear on outclk1 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk0 and outclk1, these bits are ignored and outclk1 will have inverted version of outclk0 output clock. 00: S2_B (Synthesis Engine 2, Divider B) 01: S0_C 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.
5:4	config_mux_output_2	These bits determine which clock will be selected to appear on outclk2 output in both, single ended and differential mode. 00: S2_C (Synthesis Engine 2, Divider C) 01: S0_D 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB5**
Register Name: **config_output_mux_3_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:6	config_mux_output_3	These bits determine which clock will be selected to appear on outclk3 output when in single ended mode is selected by the 'Configurable output enable and control' register. When differential mode is selected for outclk2 and outclk3, these bits are ignored and outclk3 will have inverted version of outclk2 output clock. 00: S2_D (Synthesis Engine 2, Divider D) 01: S0_D 10 and 11: reserved **Note:** Synthesizer 2 has to be enabled in register at address 0x71 whenever clock from high performance synthesizer 0 (S0) is selected to appear on the outclk in differential mode (LVPECL, LVDS, HCSL). This is not required when outclk is set to LVCMOS mode.

Register_Address: **0xB6**
Register Name: **synth3_stop_clock**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	synth3_post_div_A_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider A to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk4 at falling edge (output stays low) 11: stop outclk4 at rising edge (output stays high) . **Note:** This setting assumes that user has selected Synthesizer3 Post Divider A as the source for outclk4

Register_Address: **0xB6**
Register Name: **synth3_stop_clock**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
3:2	synth3_post_div_B_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider B to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk5 at falling edge (output stays low) 11: stop outclk5 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer3 Post Divider B as the source for outclk5
5:4	synth3_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk6 at falling edge (output stays low) 11: stop outclk6 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer3 Post Divider C as the source for outclk6
7:6	synth3_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer3 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk7 at falling edge (output stays low) 11: stop outclk7 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer3 Post Divider D as the source for outclk7

Register_Address: **0xB7**
Register Name: **synth2_stop_clock**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	synth2_post_div_A_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider A to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk0 at falling edge (output stays low) 11: stop outclk0 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider A as the source for outclk0
3:2	synth2_post_div_B_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider B to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk1 at falling edge (output stays low) 11: stop outclk1 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider B as the source for outclk1
5:4	synth2_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk2 at falling edge (output stays low) 11: stop outclk2 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider C as the source for outclk2
7:6	synth2_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer2 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop outclk3 at falling edge (output stays low) 11: stop outclk3 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer2 Post Divider D as the source for outclk3

Register_Address: **0xB8**
Register Name: **synth1_0_stop_clock**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	synth0_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer0 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk0 at falling edge (output stays low) 11: stop hpoutclk0 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer0 Post Divider C as the source for hpoutclk0
3:2	synth0_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer0 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk1 at falling edge (output stays low) 11: stop hpoutclk1 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer0 Post Divider D as the source for hpoutclk1
5:4	synth1_post_div_C_stop	Appropriate setting of these bits will cause Synthesizer1 Post Divider C to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk2 at falling edge (output stays low) 11: stop hpoutclk2 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer31 Post Divider C as the source for hpoutclk2
7:6	synth1_post_div_D_stop	Appropriate setting of these bits will cause Synthesizer1 Post Divider D to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk3 at falling edge (output stays low) 11: stop hpoutclk3 at rising edge (output stays high) **Note:** This setting assumes that user has selected Synthesizer1 Post Divider D as the source for hpoutclk3

Register_Address: **0xB9**
Register Name:**sync_fail_flag_status**
Default Value: **0x00**
Type:**StickyR**

Bit Field	Function Name	Description
0	Synth0_syncFail_flag	When high, this bit indicates that Synthesizer 0 has lost lock. If this status bit appears set after clearing Synth0_ClearSyncFail_flag (register at address 0xBA), it is indication that Synthesizer 0 has lost lock, therefore generating wrong output frequency. **Note:** This bit will be set upon power up or device reset.
1	Synth1_syncFail_flag	Same description as above but for Synth1
2	Synth2_syncFail_flag	Same description as above but for Synth2
3	Synth3_syncFail_flag	Same description as above but for Synth3
7:4	reserved	Leave as default.

Register_Address: **0xBA**
Register Name:**clear_sync_fail_flag**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	Synth0_clearSyncFail_flag	When high, this bit clears sticky Synth0_syncFail_flag. **Note:** after clearing Synth0_syncFail_flag, this bit must be set low for normal device operation
1	Synth1_clearSyncFail_flag	Same description as above but for Synth1
2	Synth2_clearSyncFail_flag	Same description as above but for Synth2
3	Synth3_clearSyncFail_flag	Same description as above but for Synth3
7:4	reserved	Leave as default.

Register_Address: **0xBF:0xC0**
Register Name:**phase_shift_s0_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s0_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer0 frequency for all clocks coming from Synthesizer0 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s0_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer0 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC1:0xC2**
Register Name:**phase_shift_s0_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s0_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer0 frequency for all clocks coming from Synthesizer0 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)

Register_Address: **0xC1:0xC2**
Register Name:**phase_shift_s0_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	quad_shift_s0_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer0 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC3**
Register Name:**xo_or_crystal_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	xo_or_crystal_sel	0: enables OSCo driver 1: disables OSCo driver Set to 1 when xo is used as master clock. Set to 0 when crystal is used as master clock.
7:1	Reserved	Leave as default

Register_Address: **0xC6**
Register Name:**Chip_revision_2**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Chip_revision_2	Chip revision number = 0b00000011 Note:also see Chip_revision bits in Register _Address: 0x00 for full chip revision information

Register_Address: **0xC7:0xC8**
Register Name:**phase_shift_s1_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s1_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer1 frequency for all clocks coming from Synthesizer1 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s1_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer1 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC9:0xCA**
Register Name:**phase_shift_s1_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s1_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer1 frequency for all clocks coming from Synthesizer1 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s1_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer1 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xCB:0xCC**
Register Name:**phase_shift_s2_postdiv_a**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s2_postdiv_a	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider A (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s2_postdiv_a	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider A. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xCD:0xCE**
Register Name:**phase_shift_s2_postdiv_b**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s2_postdiv_b	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider B (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s2_postdiv_b	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider B. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xCF:0xD0**
Register Name:**phase_shift_s2_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s2_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s2_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD1:0xD2**
Register Name:**phase_shift_s2_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s2_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer2 frequency for all clocks coming from Synthesizer2 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s2_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer2 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD3:0xD4**
Register Name:**phase_shift_s3_postdiv_a**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s3_postdiv_a	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider A (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s3_postdiv_a	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider A. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD5:0xD6**
Register Name:**phase_shift_s3_postdiv_b**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s3_postdiv_b	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider B (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s3_postdiv_b	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider B. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD7:0xD8**
Register Name:**phase_shift_s3_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s3_postdiv_c	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider C (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s3_postdiv_c	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider C. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xD9:0xDA**
Register Name:**phase_shift_s3_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	phase_shift_s3_postdiv_d	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer3 frequency for all clocks coming from Synthesizer3 Post Divider D (0: no shift, -1: delay output clock for 1 period, 1: advance output for 1 period, and so on)
15:13	quad_shift_s3_postdiv_d	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer3 Post Divider D. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xDB**
Register Name:**config_output_voltage**
Default Value: **0x0F**
Type:**R/W**

Bit Field	Function Name	Description
1:0	bank1_output_voltage	Based on provided voltage level to the configurable outputs bank 1 (outputs outclk3, outclk2, outclk1 and outclk0), customer must configure these bits to represent that voltage. 00: 1.5 V 01: 1.8 V 10: 2.5 V 11: 3.3 V These values are used for appropriate configurable outputs slew rate calculation
3:2	bank2_output_voltage	Based on provided voltage level to the configurable outputs bank 2 (outputs outclk7, outclk6, outclk5 and outclk4), customer must configure these bits to represent that voltage. 00: 1.5 V 01: 1.8 V 10: 2.5 V 11: 3.3 V These values are used for appropriate configurable outputs slew rate calculation
7:4	reserved	reserved

Register_Address: **0xDC**
Register Name:**config_output_slew_rate**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	slew_rate_outclk_1_0	Slew rate for outclk1 and outclk0. 0: medium 1: fast
1	slew_rate_outclk_3_2	Same description as above but for slew_rate_outclk_3_2
2	slew_rate_outclk_5_4	Same description as above but for slew_rate_outclk_5_4
3	slew_rate_outclk_7_6	Same description as above but for slew_rate_outclk_7_6
7:4	reserved	Leave as default

Register_Address: **0xE0**
Register Name:**gpio_function_pin0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin0_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO0 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin0_con_or_stat_sel	Selects whether GPIO0 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE1**
Register Name:**gpio_function_pin1**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin1_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO1 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin1_con_or_stat_sel	Selects whether GPIO1 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE2**
Register Name:**gpio_function_pin2**
Default Value: **0x60**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin2_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO2 control or status select' bit. The control and status table consist of 128 bits each. Default: Enable hpdiff0.

Register_Address: **0xE2**
Register Name:**gpio_function_pin2**
Default Value: **0x60**
Type:**R/W**

Bit Field	Function Name	Description
7	gpio_pin2_con_or_stat_sel	Selects whether GPIO2 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE3**
Register Name:**gpio_function_pin3**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin3_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO3 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin3_con_or_stat_sel	Selects whether GPIO3 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE4**
Register Name:**gpio_function_pin4**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin4_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO4 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin4_con_or_stat_sel	Selects whether GPIO4 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE5**
Register Name:**gpio_function_pin5**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin5_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO5 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin5_con_or_stat_sel	Selects whether GPIO5 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE6**
Register Name:**gpio_function_pin6**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin6_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO6 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin6_con_or_stat_sel	Selects whether GPIO6 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE7**
Register Name:**gpio_function_pin7**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin7_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO7 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused.
7	gpio_pin7_con_or_stat_sel	Selects whether GPIO7 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE8**
Register Name:**gpio_function_pin8**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin8_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO8 control or status select' bit. The control and status table consist of 128 bits each. Deafault: GPIO unused.
7	gpio_pin8_con_or_stat_sel	Selects whether GPIO8 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE9**
Register Name:**gpio_function_pin9**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin9_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO9 control or status select' bit. The control and status table consist of 128 bits each. Deafault: GPIO unused.
7	gpio_pin9_con_or_stat_sel	Selects whether GPIO9 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xEA**
Register Name:**gpio_function_pin10**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin10_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO10 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused
7	gpio_pin10_con_or_stat_sel	Selects whether GPIO10 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xEB**
Register Name:**gpio_function_pin11**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	gpio_pin11_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO11 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO unused
7	gpio_pin11_con_or_stat_sel	Selects whether GPIO11 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xF7**
Register Name:**spurs_suppression**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	spurs_suppression	This register is used for spurs suppression. Depending on the synthesizer configuration GUI will generate recommended value. Please refer to GUI for recommended value that should be written to this register. When the spurs_supression register is changed, the ZL30230 requires 200msec to reconfigure itself, no reads or writes to the device are permitted during this reconfiguration period. The spurs_suppression register should only be written with values recommended by the ZL30230 GUI and it should only be written if a 24.576MHz master clock oscillator or crystal resonator is being used

9.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD-IO} AV_{DD}	3.135	3.30	3.465	V
2	Core supply voltage	V_{CORE}	1.71	1.80	1.89	V
3	Operating temperature	T_A	-40	25	85	°C
4	Input voltage	V_{DD-IO}	2.97	3.30	3.63	V
5	I/O Bank Supply Voltage	$B1V_{DD-IO}$, $B2V_{DD-IO}$	1.425 1.71 2.375 3.135	1.5 1.8 2.5 3.3	1.575 1.89 2.625 3.465	V

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Power - Core

	Characteristics	Sym.	Typ.	Max.	Units	Notes
1	Core supply current (Vcore)	I_{CORE} (Vdd 3.3V)	46	48	mA	
		I_{CORE} (Vdd 1.8V)	102	109	mA	
2	Current for each HP Synthesis Engine	I_{SYN} (Vdd 3.3V)	57	73	mA	
		I_{SYN}(Vdd 1.8V)	0.2	1	mA	
3	Current for each General Purpose Synthesis Engine	I_{SYN} (Vdd 3.3V)	4	7	mA	
		I_{SYN}(Vdd 1.8V)	12	13	mA	

DC Electrical Characteristics - Power - High Performance Outputs

	Characteristics	Sym.	Typ.	Max.	Units	Notes
1	Power for each hpdiff clock driver	P_{hpdiff}(Vdd 3.3V)	85	91	mW	Including power to biasing and load resistors R_L = 50Ω
2	Power for each hpdiff clock driver minus power dissipated in the biasing and load resistors.	P_{hpdiff}(Vdd 3.3V)	36	42	mW	Without power to biasing and load resistors R_L = 50Ω
3	Power for each hpdiff clock driver (reduced power mode)	$P_{hpdifflp}$(Vdd 3.3V)	80	86	mW	Including power to biasing and load resistors R_L = 50Ω
4	Power for each hpdiff clock driver minus power dissipated in the load resistor. (reduced power mode)	$P_{hpdifflp}$(Vdd 3.3V)	31	37	mW	Without power to biasing and load resistors R_L = 50Ω
5	Power for each output divider of high performance synthesizers (enabled if one of two differential outputs assigned to it is enabled).	P_{div}(Vdd 3.3V)	17	40	mW	
6	Power for each hpoutclk clock driver	P_{hpout}(Vdd 3.3V)	17+ 7	40+36	mW	155.52 MHz output 10 pF load fixed power (due to output divider) + variable power (proportional to freqeuncy and load)

DC Electrical Characteristics * - Power - Configurable Outputs

	Characteristics	Sym.	Typ.	Max.	Units	Notes
1	Power for each outclk clock driver in LVDS mode	$P_{Out-LVDS}$	32	35	mW	Including power to load resistor R_L = 100Ω
2	Power for each LVDS clock driver minus power dissipated in the load resistor	$P_{Out-LVDS}$	31	34	mW	Without power to load resistor R_L = 100Ω
3	Power for each outclk clock driver in LVPECL mode	$P_{Out-LVPECL}$	80	81	mW	Including power to biasing and load resistors R_L = 50Ω
4	Power for each LVPECL clock driver minus power dissipated in the biasing and load resistors	$P_{Out-LVPECL}$	38	39	mW	Without power to biasing and load resistors R_L = 50Ω
5	Power for each outclk clock driver in HCSL mode	$P_{Out-HCSL}$	62	64	mW	Including power to load resistors R_L = 33Ω + 50Ω
6	Power for each HCSL clock driver minus power dissipated in the load resistors	$P_{Out-HCSL}$	46	48	mW	Including power to load resistors R_L = 33Ω + 50Ω
7	Power for each outclk clock driver in 1.5V CMOS mode	$P_{Out-CMOS1.5}$	5.9	6.2	mW	C_L = 10pF @155.52MHz (proportional to freqeuncy and load)
8	Power for each outclk clock driver in 1.8V CMOS mode	$P_{Out-CMOS1.8}$	9	10	mW	C_L = 10pF @155.52MHz (proportional to freqeuncy and load)
9	Power for each outclk clock driver in 2.5V CMOS mode	$P_{Out-CMOS2.5}$	23	24	mW	C_L = 10pF @155.52MHz (proportional to freqeuncy and load)
10	Power for each outclk clock driver in 3.3V CMOS mode	$P_{Out-CMOS3.3}$	42	44	mW	C_L = 10pF @155.52MHz (proportional to freqeuncy and load)

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise state.

DC Electrical Characteristics - Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	$0.7 \cdot V_{DD-IO}$			V	
2	CMOS low-level input voltage	V_{CIL}			$0.3 \cdot V_{DD-IO}$	V	
3	CMOS Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V

AC/DC Electrical Characteristics - OSCi Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	2.0			V	
2	CMOS low-level input voltage	V_{CIL}			0.8	V	
3	Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Duty Cycle		40		60	%	

DC Electrical Characteristics - High Performance Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPCMOS High-level output voltage	V_{OH}	$0.8 \cdot AV_{DD}$			V	I_{OH} = 2mA C_L = 5pF
2	HPCMOS Low-level output voltage	V_{OL}			$0.2 \cdot AV_{DD}$	V	I_{OL} = 2mA C_L = 5pF
3	LVPECL: High-level output voltage	V_{OH_LVPECL}	AV_{DD} - 1.12	AV_{DD} - 1.00	AV_{DD} - 0.88	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
4	LVPECL: Low-level output voltage	V_{OL_LVPECL}	AV_{DD} - 1.81	AV_{DD} - 1.71	AV_{DD} - 1.55	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
5	LVPECL: Differential output voltage*	V_{OD_LVPECL}	0.53	0.67	0.80	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF

* Output swing is guaranteed for frequency up to 720MHz, it may decrease by 50mv if the frequency is greater than 720 MHz

DC Electrical Characteristics - Configurable Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	3.3V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{D\,D\text{-}IO}$ $0.8 \cdot B2V_{D\,D\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
2	3.3V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\,\text{-}IO}$ $0.2 \cdot B2V_{DD\,\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
3	2.5V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{D\,D\text{-}IO}$ $0.8 \cdot B2V_{D\,D\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
4	2.5V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\,\text{-}IO}$ $0.2 \cdot B2V_{DD\,\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
5	1.8V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{D\,D\text{-}IO}$ $0.8 \cdot B2V_{D\,D\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
6	1.8V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\,\text{-}IO}$ $0.2 \cdot B2V_{DD\,\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
7	1.5V CMOS High-level output voltage	V_{OH}	$0.8 \cdot B1V_{D\,D\text{-}IO}$ $0.8 \cdot B2V_{D\,D\text{-}IO}$			V	I_{OH} = 2mA C_L = 5pF
8	1.5V CMOS Low-level output voltage	V_{OL}			$0.2 \cdot B1V_{DD\,\text{-}IO}$ $0.2 \cdot B2V_{DD\,\text{-}IO}$	V	I_{OL} = 2mA C_L = 5pF
9	LVPECL: High-level output voltage	$V_{OH\_LV\,PECL}$	AV_{DD} - 1.12	AV_{DD} - 1.00	AV_{DD} - 0.88	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
10	LVPECL: Low-level output voltage	$V_{OL\_LV\,PECL}$	AV_{DD} - 1.81	AV_{DD} - 1.71	AV_{DD} - 1.55	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
11	LVPECL: Differential output voltage	$V_{OD\_LV\,PECL}$	0.48	0.64	0.80	V	R_L = 50Ω to AV_{DD} - 2V, C_L = 1pF
12	LVDS: High-level output voltage	$V_{OH\_LV\,DS}$	1.18	1.30	1.47	V	R_L = 100Ω, C_L = 1pF
13	LVDS: Low-level output voltage	$V_{OL\_LV\,DS}$	0.91	0.98	1.10	V	R_L = 100Ω, C_L = 1pF

DC Electrical Characteristics - Configurable Outputs

14	LVDS: Differential output voltage	V_{OD_LVDS}	0.27	0.32	0.37	V	R_L = 100Ω, C_L = 1pF
15	LVDS: output offset voltage	V_{OFF_LVDS}		30		mV	R_L = 100Ω, C_L = 1pF
16	HCSL: High-level output voltage	V_{OH_HCSL}	0.6	0.7	0.9	V	R_L = 50Ω each to ground C_L = 5pF
17	HCSL: Low-level output voltage	V_{OL_HCSL}	0.00	0.01	0.03	V	R_L = 50Ω each to ground C_L = 5pF

AC Electrical Characteristics* - Output Timing Parameters Measurement Voltage Levels (see Figure 24)

	Characteristics	Sym.	CMOS	LVPECL	LVDS	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$ $V_{T\text{-}CML}$	$0.5V_{DD}$	$0.5V_{OD\_LVPECL}$	$0.5V_{OD\_CML}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	$0.8V_{OD\_LVPECL}$	$0.8V_{OD\_CML}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	$0.2V_{OD\_LVPECL}$	$0.2V_{OD\_CML}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions
* Voltages are with respect to ground (GND) unless otherwise stated

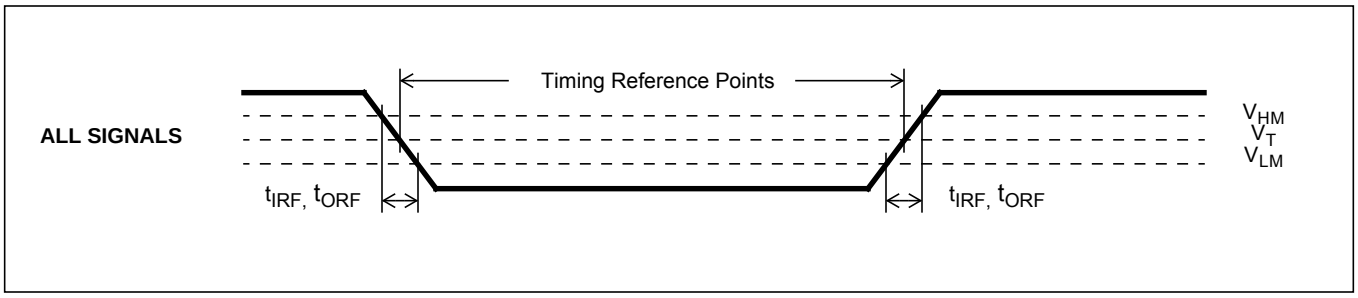


Figure 24 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Outputs (see Figure 25).

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Clock skew between high performance outptus	$t_{OUT2OUTD}$	-1	0	1	ns	
2	Clock skew between configurable outputs	$t_{OUT2OUTD}$		0		ns	
3	Output clock Duty Cycle	t_{PWH}, t_{PWL}	45%	50%	55%	Duty Cycle	
4	hpdiff (LVPECL) Output clock rise or fall time	t_r / t_f	265	370	515	ps	
5	hpoutclk (LVCMOS) clock rise and fall time	t_r / t_f	620	950	1490	ps	10pF load
6	Output Clock Frequency (hpdiff)	F_{hpdiff}			750	MHz	
7	Output Clock Frequency (hpoutclk)	F_{hpout}			177.5	MHz	
8	Output Clock Frequency (single-ended configurable outclk outputs)	F_{out}			160	MHz	
9	Output Clock Frequency (differential configurable outclk outputs)	F_{out_diff}			350	MHz	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

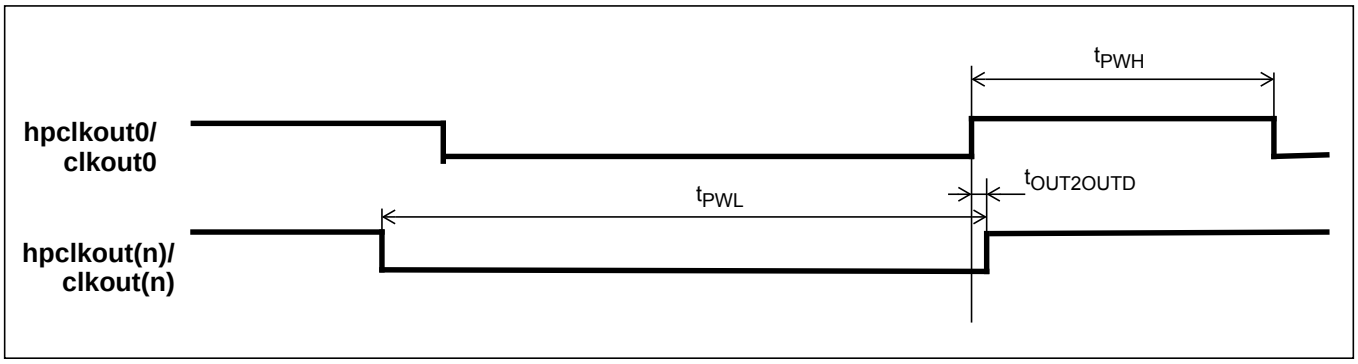


Figure 25 - Output Timing Referenced To hpclkout0/clkout0

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 26, and Figure 27 describe the MSB first mode. Table 6 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 6 - Serial Peripheral Interface Timing

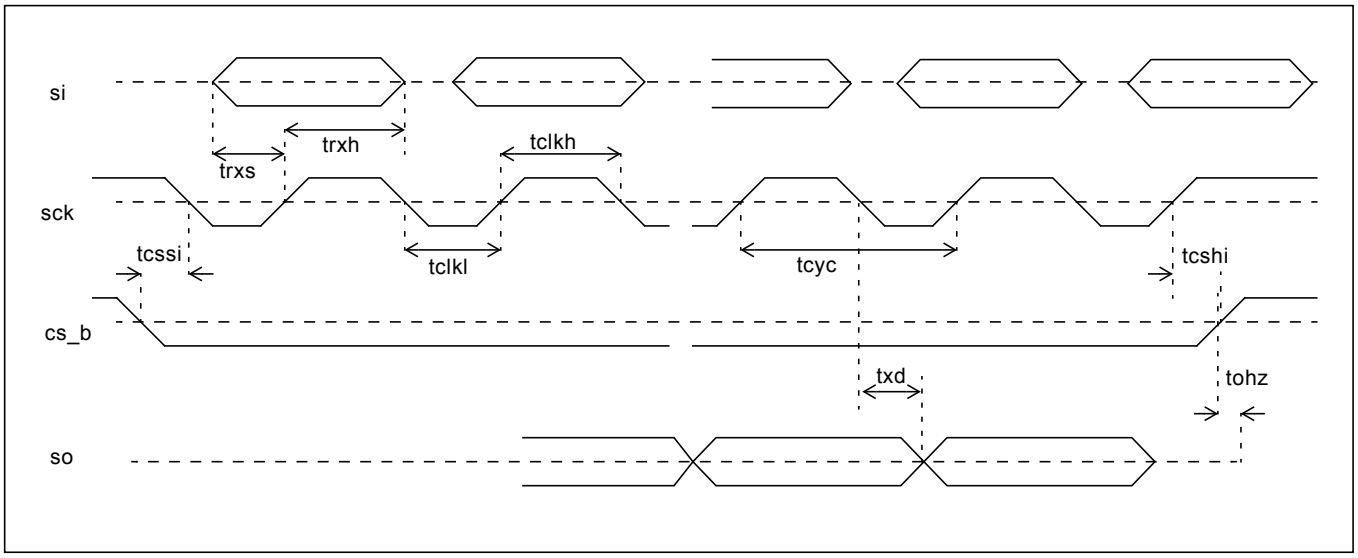


Figure 26 - Serial Peripheral Interface Timing - LSB First Mode

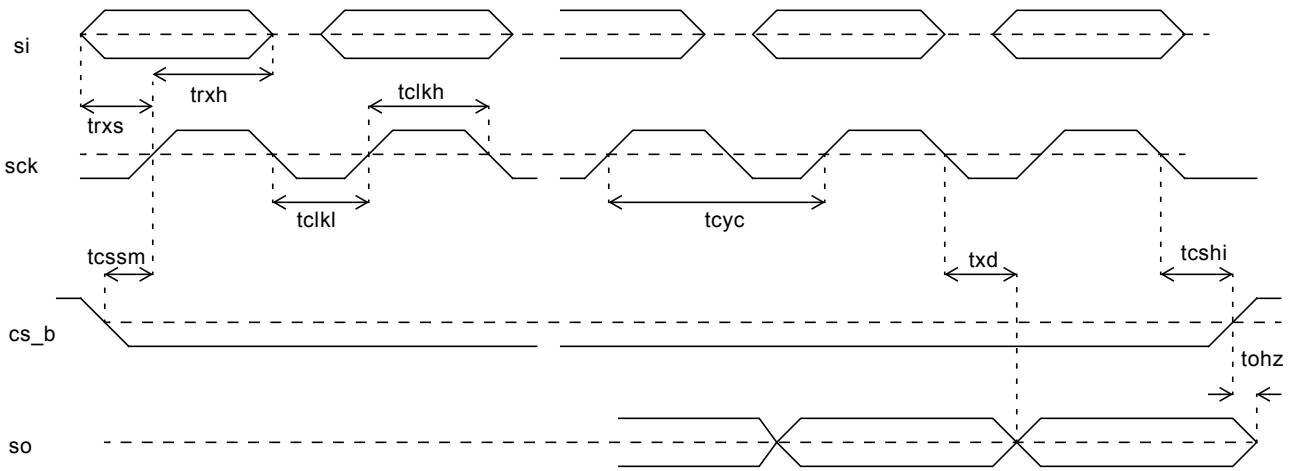


Figure 27 - Serial Peripheral Interface Timing - MSB First Mode

The timing specification for the I^2C interface is shown in Figure 28 and Table 7.

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by choice of pull-up resistor
Fall time	t_f	20 + $0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 7 - I^2C Serial Microport Timing

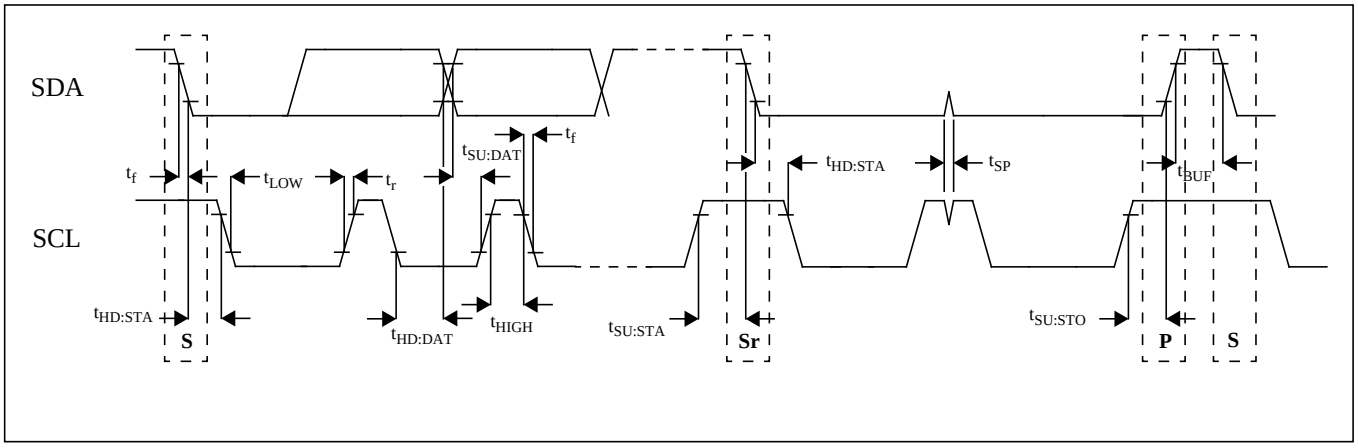


Figure 28 - I^2C Serial Microport Timing

10.0 Performance Characterization

10.1 Output Clocks RMS Jitter Generation

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
622.08 MHz	50kHz - 80MHz	0.63	ps_{rms}	
	12kHz - 20MHz	0.72	ps_{rms}	

Table 8 - Jitter Generation Specifications - HPDIFF Outputs

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12KHz - 5MHz	0.99	ps_{rms}	
77.76 MHz	12KHz - 20MHz	1.04	ps_{rms}	
125 MHz	12KHz - 20MHz	0.85	ps_{rms}	
156.25 MHz	12KHz - 20MHz	0.92	ps_{rms}	

Table 9 - Jitter Generation Specifications - HPOUT Outputs

Output Frequency	Jitter Measurement Filter	Typ	Max.	Units	Notes
25 MHz	12KHz - 5MHz	2.7	TBD	ps_{rms}	
77.76 MHz	12KHz - 20MHz	1.7	TBD	ps_{rms}	
125 MHz	12KHz - 20MHz	2.8	TBD	ps_{rms}	
156.25 MHz	12KHz - 20MHz	4.2	TBD	ps_{rms}	

Table 10 - Jitter Generation Specifications - Configurable Outputs driven from High Performance Synthesizers - Differential Mode

Output Frequency	Jitter Measurement Filter	Typ	Max.	Units	Notes
25 MHz	12KHz - 5MHz	13.1	TBD	ps_{rms}	
77.76 MHz	12KHz - 20MHz	14.3	TBD	ps_{rms}	
125 MHz	12KHz - 20MHz	14.9	TBD	ps_{rms}	
156.25 MHz	12KHz - 20MHz	14.7	TBD	ps_{rms}	

Table 11 - Jitter Generation Specifications - Configurable Outputs driven from General Purpose Synthesizers - Differential Mode

10.2 Output Clocks Cycle-to-Cycle Jitter Generation

Output Frequency	Max.	Units	Notes
125 MHz	29.2	ps_{PK-PK}	
156.25 MHz	28.2	ps_{PK-PK}	
212.5 MHz	27.9	ps_{PK-PK}	

Table 12 - Jitter Generation Specifications - HPDIFF Outputs

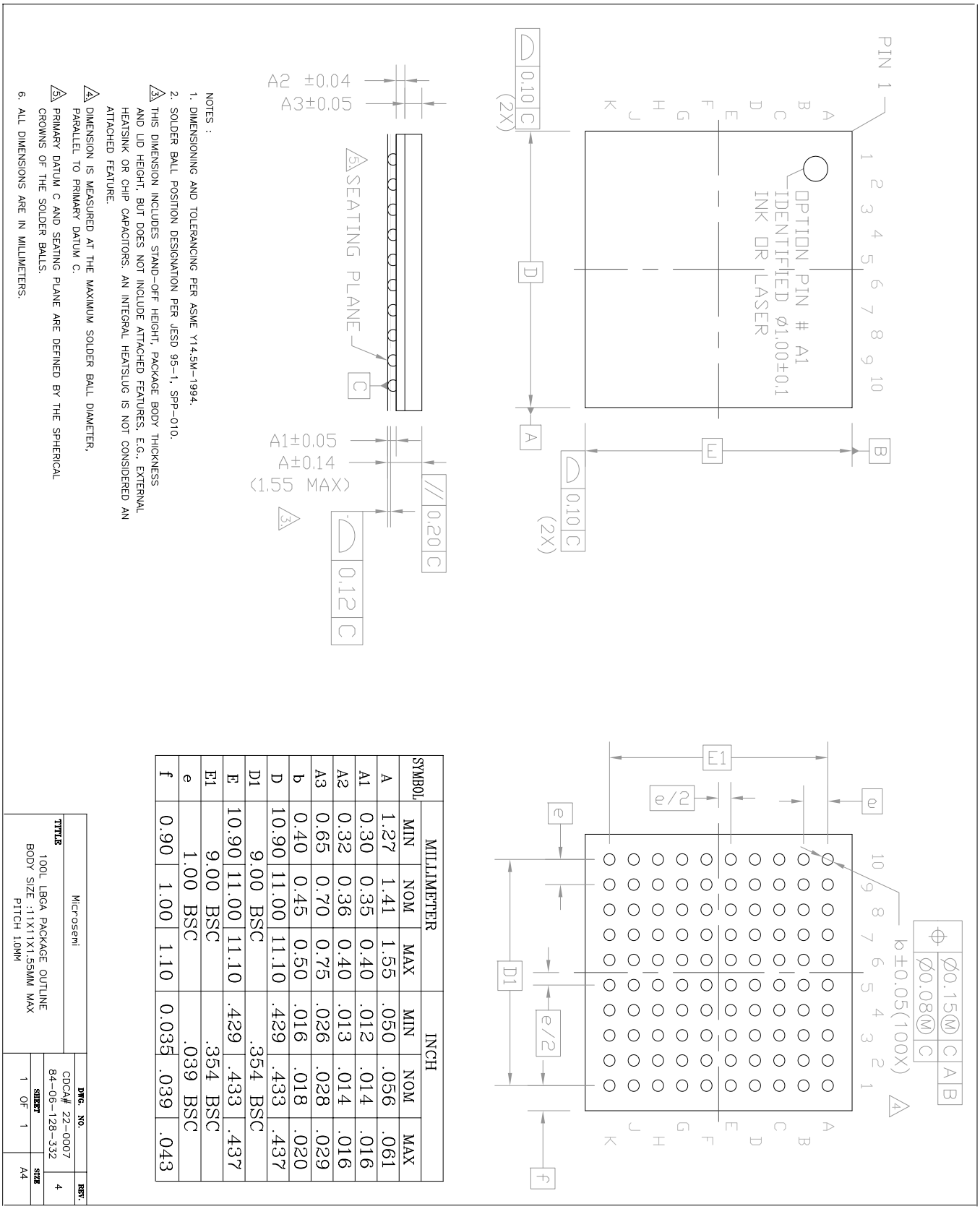
11.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air 1 m/s 2 m/s	29.7 26.5 25.3	$^oC/W$
Junction to Case Thermal Resistance	θ_{jc}		7.7	$^oC/W$
Maximum Junction Temperature *	T_{jmax}		125	^oC
Maximum Ambient Temperature	T_A		85	^oC

* Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded

Table 13 - Thermal Data

12.0 Mechanical Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.27	1.41	1.55	.050	.056	.061
A1	0.30	0.35	0.40	.012	.014	.016
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.65	0.70	0.75	.026	.028	.029
b	0.40	0.45	0.50	.016	.018	.020
D	10.90	11.00	11.10	.429	.433	.437
D1		9.00 BSC			.354 BSC	
E	10.90	11.00	11.10	.429	.433	.437
E1		9.00 BSC			.354 BSC	
e		1.00 BSC			.039 BSC	
f	0.90	1.00	1.10	0.035	.039	.043

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Microsemi		DWG. NO.	REV.
TITLE: 100L LBGA PACKAGE OUTLINE BODY SIZE :11X11X1.55MM MAX PITCH 1.0MM		CDCA# 22-0007 84-06-128-332	4
		SIZE	
		A4	
		SHEET 1 OF 1	

13.0 Package Markings

13.1 100-pin BGA. Package Top Mark Format

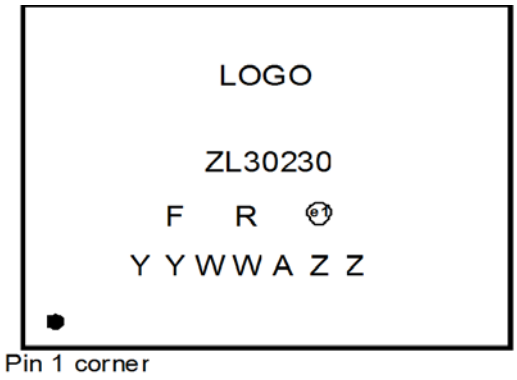


Figure 29 - Non-customized Device Top Mark

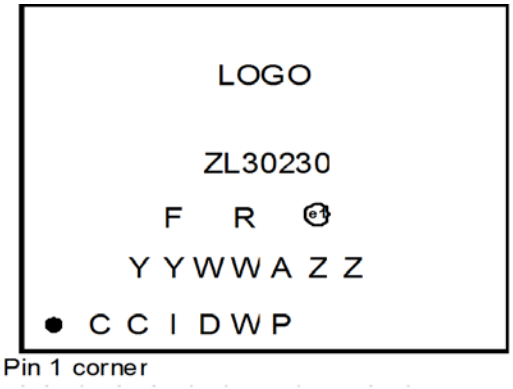


Figure 30 - Custom Factory Programmed Device Top Mark

Line	Characters	Description
1	ZL30230	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

Table 14 - Package Marking Legend

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